TM 9-5000-13
15 May 1956

CHAPTER 4

AUTOMATIC ZERO SETTING CONTROLS

Section I. OVER-ALL PURPOSE

51. GENERAL

The purpose of the automatic zero set unit is threefold. First, it reduces the initial offset voltage error of the DC amplifier. Second, it continuously compensates for the slow drift in the DC amplifier. Third, it improves the computing accuracy and helps to decrease the mathematical error by increasing the gain, K, of the DC amplifier.

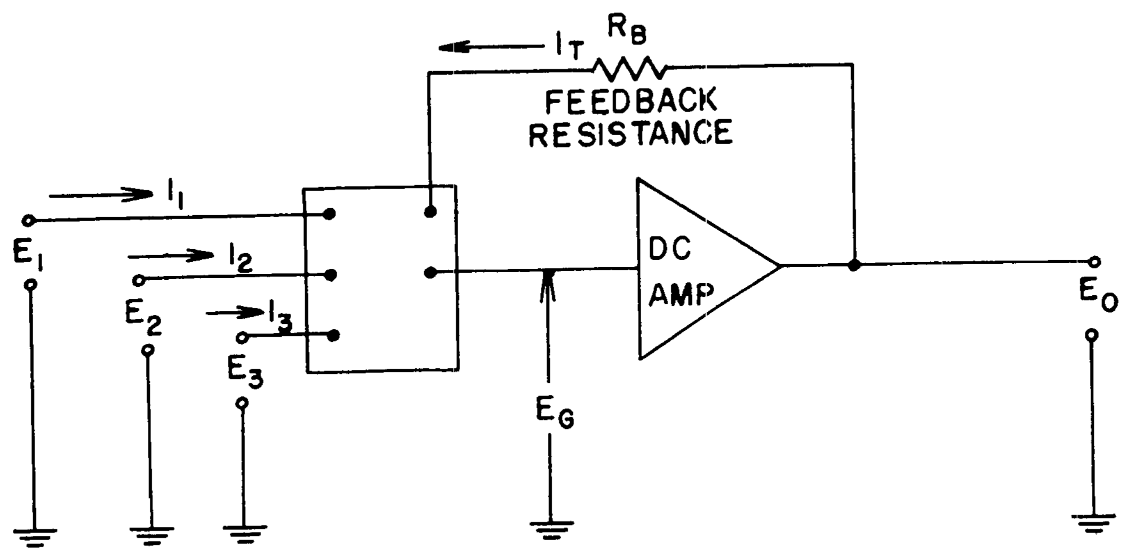

Figure 37. Summing amplifier circuit.

52. COMPUTER ERRORS

In all of the mathematical operations performed by the DC amplifier and its associated input circuit, the voltage e_g existing between the grid of the first stage and ground is made to approach zero. Figure 37 illustrates the manner in which the DC amplifier nulls the voltage for a summing circuit. The DC amplifier maintains a current flow, I_T, through feedback resistor R_B that is equal to the sum of the input currents I_1, I_2, and I_3. If I_T does not equal the sum of the input currents, an error voltage e_g will exist between the input signal grid and ground. Any deviation of e_g from zero constitutes an error in

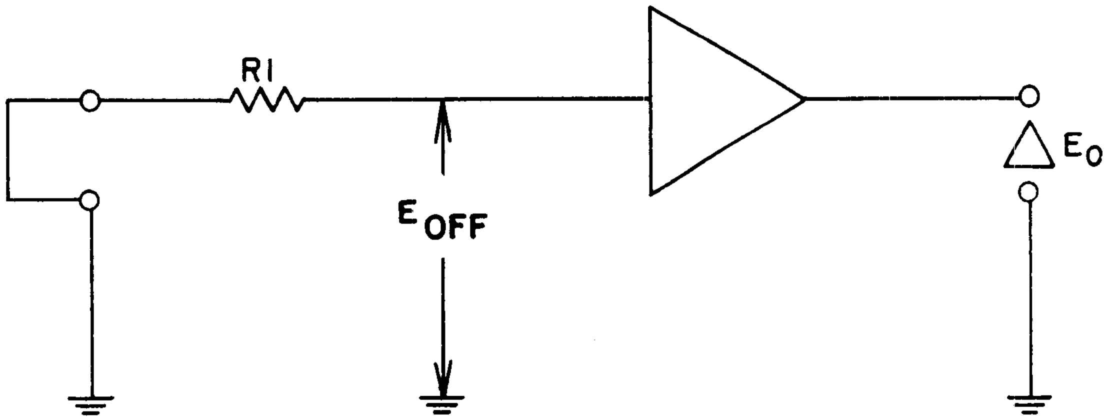

Figure 38. Illustration of offset voltage.

the computing function, because the output voltage E_0 does not represent a perfect reproduction of the input signal voltages. The zero offset voltage is, by definition, the voltage which exists at the output terminals of a DC amplifier having no feedback path when the input terminals to the network are grounded (fig 38). The zero offset voltage e_0 is expressed by the equation:

$$e_{off} = \frac{e_0}{-K} . \qquad (10)$$

Where e_{off} is the offset voltage existing between the input signal grid and ground; e_0 is the zero offset voltage existing at the DC amplifier output; and -K is the gain of the DC amplifier. The zero offset voltage, one of the greatest handicaps in the use of DC amplifiers, consists of two components: initial offset voltage, and drift voltage. The initial offset voltage is the voltage arising from manufacturing variations in tubes and components so that the operating conditions differ from one unit to another. Therefore, it is impractical to build the amplifiers so that they will give zero output with zero input. The drift voltage is the offset voltage caused by the slow change of the circuit parameters due to heating, aging, variations in the plate and filament voltage supply, and by changes in the vacuum tube characteristics caused by heating, vibration, shocks, and thermal effects. There is another type of error which is quite distinct and completely separate from zero offset voltage error. It is called the mathematical error. In any DC computing circuit with feedback (fig 37) this error is present because the computing circuit does not perform the exact mathematical operation. Eliminating any offset voltage error, the feedback current still does not exactly equal the signal input current. The mathematical voltage error at the input grid to ground is designated by $e = \frac{-E_0}{K}$ where E_0 is the output signal voltage, and K is the interval gain of

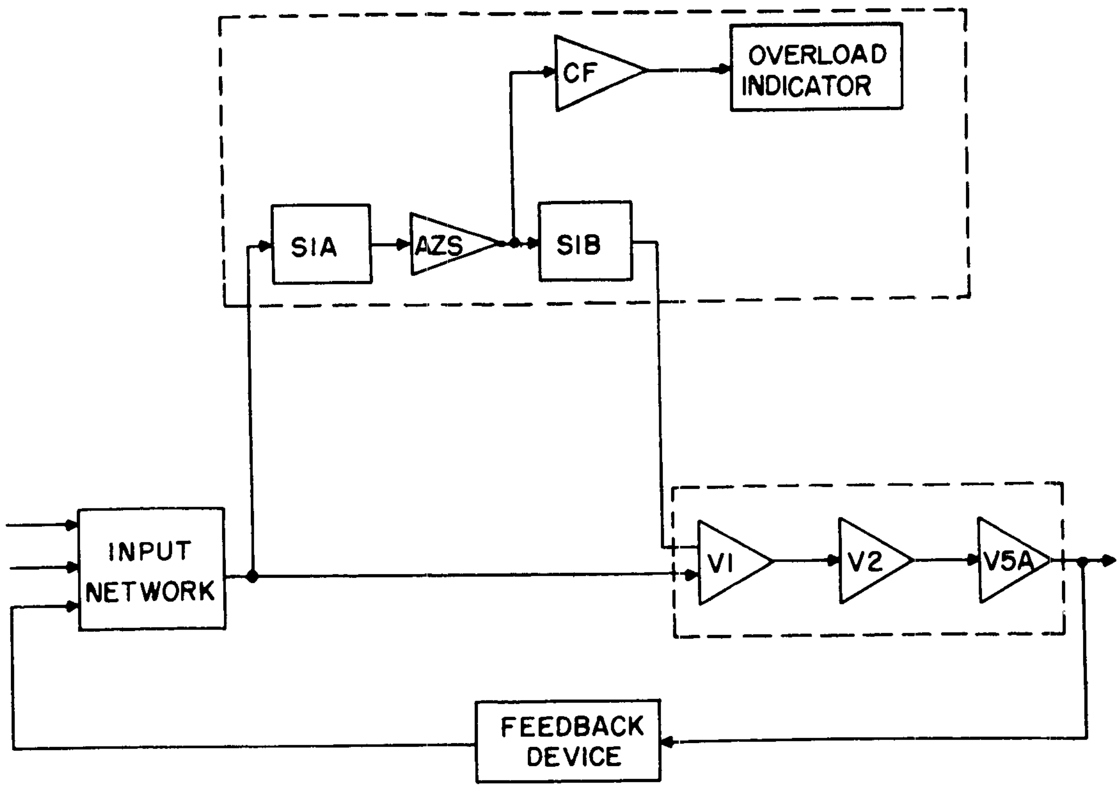

Figure 39. Automatic zero setting, typical block diagram.

the amplifier. Error voltage e_g on the signal grid consists partly of the offset voltage e_{off} and partly of the mathematical error voltage e. If e_g were reduced to zero, the output voltage E_0 would be a perfect reproduction of the input voltages to the DC amplifier. By increasing the gain of the DC amplifier, the magnitude of the error voltage e_g will be decreased.

53. PRINCIPLES OF AUTOMATIC ZERO SETTING (fig 39)

The DC amplifier is a 3-stage amplifier having a balanced twin triode first stage with a common cathode resistor. The total error caused by the offset error and the mathematical error manifests itself at the summing point, the grid of V1A. The basic purpose of the automatic zero setting system is to reduce the error voltage on the grid of V1A to zero. A positive error is taken for an example. This positive error is sent through an a-c amplifier, its polarity is reversed, and it is applied as a negative voltage to the correction grid of V1B. The reduction in plate current through tube V1B causes the common cathode potential to go in a negative direction. This effect is the same as if the grid of V1A had become more positive; therefore, tube V1A draws more current, its plate voltage drops, and this negative-going signal is sent through tubes V2 and V5A. The signal output, in this example, has become more negative, and the feedback to the grid of V1A is more negative. This larger negative feedback tends to cancel the original positive error voltage. This readjustment continues until the error voltage is zero. Any attempt to amplify this d-c voltage in the AZS amplifier would be met by the same difficulties as in the DC amplifier. Therefore, the automatic zero set (AZS) amplifier is an a-c amplifier. Since an a-c amplifier does not respond to steady d-c signals, the voltage is chopped by a rotary switch before amplification. The output of the AZS amplifier is reversed in polarity. It is demodulated by the other half of the rotary switch. This method of demodulation is known as synchronous switching. The output of the AZS amplifier is stored on capacitor C3 (fig 39) attached to the correction grid of the DC amplifier. The closer the signal input grid voltage approaches zero, the more precisely the output of the DC amplifier approaches the desired function of the input. In other words, the more precise the zero setting, the more accurate the DC amplifier. However, the precision of zero setting is dependent upon and is directly proportional to the amplification in the automatic zero set circuit. In the Nike I computer, there are two types of automatic zero setting systems. One is called the precision automatic zero set system, and is used where more stringent requirements on computing accuracy are needed. The other type is the semiprecision automatic zero set system, and it is used where less computing accuracy is required. Since the precision AZS system requires greater computing accuracy, a greater amount of amplification is needed.

54. COMPONENTS (TM 9-5000-26)

a. The DC amplifier to be zero set.

b. The zero set switch and network GS15640 (page 27) or switch and network GS15557, (page 28).

c. AZS amplifier GS15641, (page 29). This is an a-c amplifier with one stage of amplification followed by a double cathode follower for overload indicator circuits.

55. TYPICAL BLOCK DIAGRAM

One AZS switch has either 12 or 6 possible configurations for completing a zero set circuit, depending upon whether it is a semiprecision or a precision switch. The switch connects the DC amplifier and its input network and feedback device across the AZS amplifier.

Section II. SEMIPRECISION AUTOMATIC ZERO SET SYSTEM

56. GENERAL (TM 9-5000-26)

The purpose of the semiprecision AZS system is to reduce the initial offset voltage error continuously, to compensate for the slow drift in the DC amplifier, and to improve the computing accuracy and decrease the mathematical error by increasing the gain of the DC amplifier. The automatic zero set switches are located in the center of the equipment frame in the computer amplifier cabinet assembly (pages 4 and 5). ZS groups 1 and 5 are precision AZS switches, and ZS groups, 2, 3, 4, 6, 7, and 8 are semiprecision AZS switches. The AZS a-c amplifiers for each group are located directly below their respective switches. The meters at the top of the cabinet display the magnitudes of the voltages present at the outputs of the amplifiers in the computer (page 29A7 and D7). Meters M1 and M2 (page 5) are meters M19 and M319 respectively on page 29 . There are two zero check switches on the center post of the amplifier cabinet. Operating these switches removes all inputs to the amplifiers. A check can then be made of all amplifiers to see if any amplifier has a zero offset voltage or is drifting.

57. DETAILED FUNCTIONAL OPERATION (TM 9-5000-26)

The operation of the semiprecision automatic zero set system is shown on page 26C1 to C5 This example shows the AZS system used in conjunction with the $+X_M$ amplifier. A lead from the signal grid of V1A of the $+X_M$ amplifier is connected to the zero set net at A4. (Note 2 indicates specific terminals or apparatus identified in the tabulations. The $+X_M$ amplifier is in semiprecision group 2, switch channel 2 (page 26B6). (All the other amplifiers are similarly tabulated.) The error signal enters the rotary switch S1A at contact 4. The contact arm of the AZS switch is revolving and makes contact at each point at a rate of five times per second. As the rotary arm revolves, it makes contact with pin 1, which is at ground potential, pin 2, which is connected (in this group) to the $-X_M$ DC amplifier, pin 3, which is grounded, pin 4, which is connected to the $+X_M$ DC amplifier, and so on through 24 contacts. The odd-numbered contacts are all grounded to permit the AZS amplifier to return to its quiescent state between each operation. This prevents any offset error voltage of one DC amplifier from being applied to the next DC amplifier which is being zero set. The even numbered contacts receive the error signal from each of 12 different DC amplifiers in sequence as the brush arm makes contact. When the brush arm contacts pin 4 on the left side of AZS switch S1A (C2), the $+X_M$ signal grid is connected to the outer ring of the rotary switch and from the ring to the signal grid of the AZS a-c amplifier. The error signal is amplified and reversed in polarity and passes through a coupling capacitor to the outer ring of S1B. Since the opposite roller of the brush arm is in contact with pin 4 of S1B, the correction signal is connected to the correction grid of V1B in the $+X_M$ DC amplifier. Assume that the error signal on the grid of V1A in figure 39 is positive. It is amplified and reversed in polarity in the AZS amplifier, and the negative correction signal is applied to the correction grid of V1B. This negative voltage on the grid of V1B reduces the plate current flow in the tube, thus causing the voltage on the common cathode resistor to change in a negative direction. Tube V1A draws more plate current, its plate voltage changes in a negative direction, and this negative-going signal is amplified by V2 and V5A. This signal is negative at the output of the DC amplifier; therefore, the feedback voltage to the grid of V1A is more negative. This negative feedback tends to reduce the positive error signal at the input to the DC amplifier to zero. The over-all gain of the AZS circuit depends not only upon the gain, K, of the AZS amplifier, but also upon all of the associated circuit elements (C1, C3, and R3) and the speed of rotation of the rotary switch. The over-all gain of the AZS circuit is 200 (46 db). When the AZS circuit is connected to the signal grid of the DC amplifier, the AZS circuit multiplies the gain of the DC amplifier by 200. At coordinates 26C5 of 2y are a 1-megohm resistor and a 1-microfarad capacitor. In the $+X_M$ DC amplifier circuit, these are R83 and C80B (26C6), which are used as an integrating network. When the brush of the rotary switch is not in contact with the $+X_M$ amplifier, the grid voltage of V1B is maintained at a level by R83 and C80B. Without this circuit, conduction of V1A would drop as S1B moved away from contact 4. The amplifier would be unbalanced, and an error would be generated. The purpose and use of the overload indicator will be covered later.

58. MECHANICAL OPERATION

There are 6 semiprecision zero set switches and 2 precision zero set switches to zero set 76 DC amplifier, +250-volt regulator, and the +S voltage amplifier. The +S voltage (106.667 volts) is used in the computer for an accurate slant range measurement. If this voltage is incorrect, then all of the computations and scale factors in the computer will be wrong. The +S voltage amplifier is zero set to prevent drifting. Each semiprecision zero set switch handles 12 DC amplifiers, except group 4, which handles 5. Each precision zero set switch handles six DC amplifiers (page 26A6, A7, and A8). The typical semiprecision zero set circuit on page 26C2 and C4 shows the electrical connections of switch S1 correctly, but it is misleading as to mechanical operation. Figure 40 indicates that each of the contacts is a movable pin. The odd-numbered pins are connected to ground. Each even-numbered contact pin of S1A is connected to the V1A grid of a different DC amplifier. The even-numbered contacts of S1B are connected to the V1B grid of the corresponding DC amplifier. Closely spaced behind all the pins of S1A is a semicircular

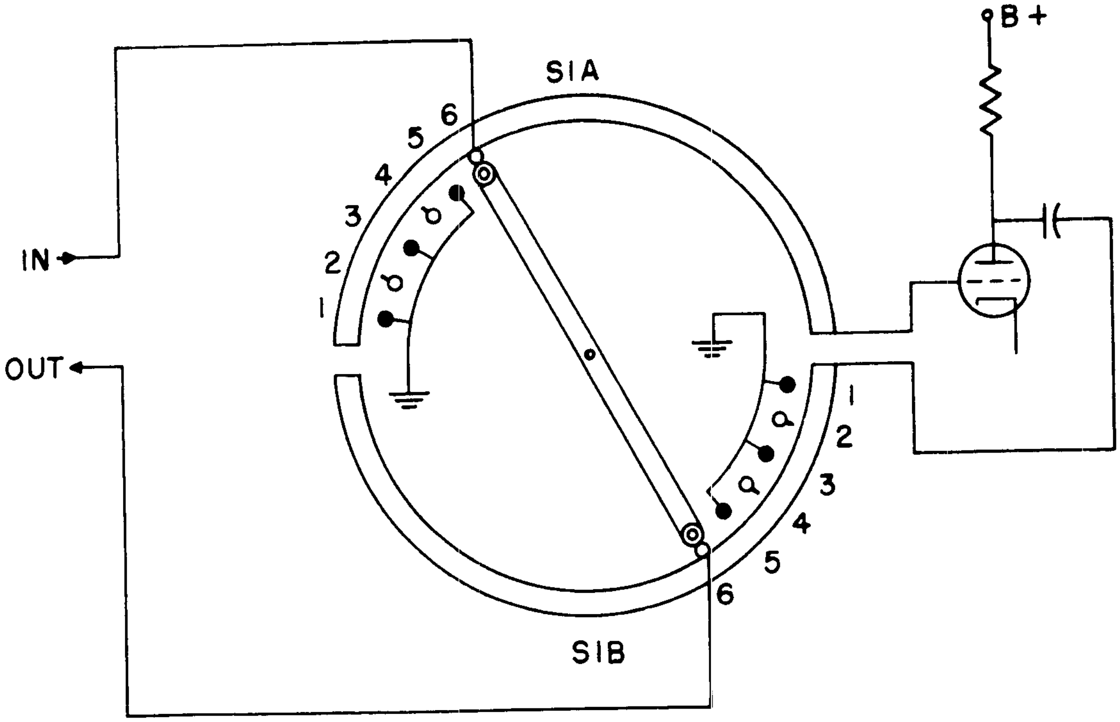

Figure 40. Mechanics of the semiprecision automatic zero set switch.

metal contact that is electrically connected to the grid of the AZS amplifier. A similar metal contact is spaced directly behind the pins of S1B. The rotary switch arms are nonconductors, pivoted in the center, with insulated rollers at each end. These rollers push the contact pins, one at a time, back against the semicircular ring to make the connection. A 2-phase induction motor rotates the arms of the switch at about 155 rpm. Effectively, the speed is 310 rpm because there are two arms on the rotary switch. Each amplifier is zero set about five times per second. Mechanical and physical limitations and space considerations dictate the speed of the brush arms. Most important, the AZS switch chops the d-c error signal into a function resembling a square wave so that the AZS a-c amplifier can amplify it. The reason for using an a-c amplifier is stated in paragraph 53.

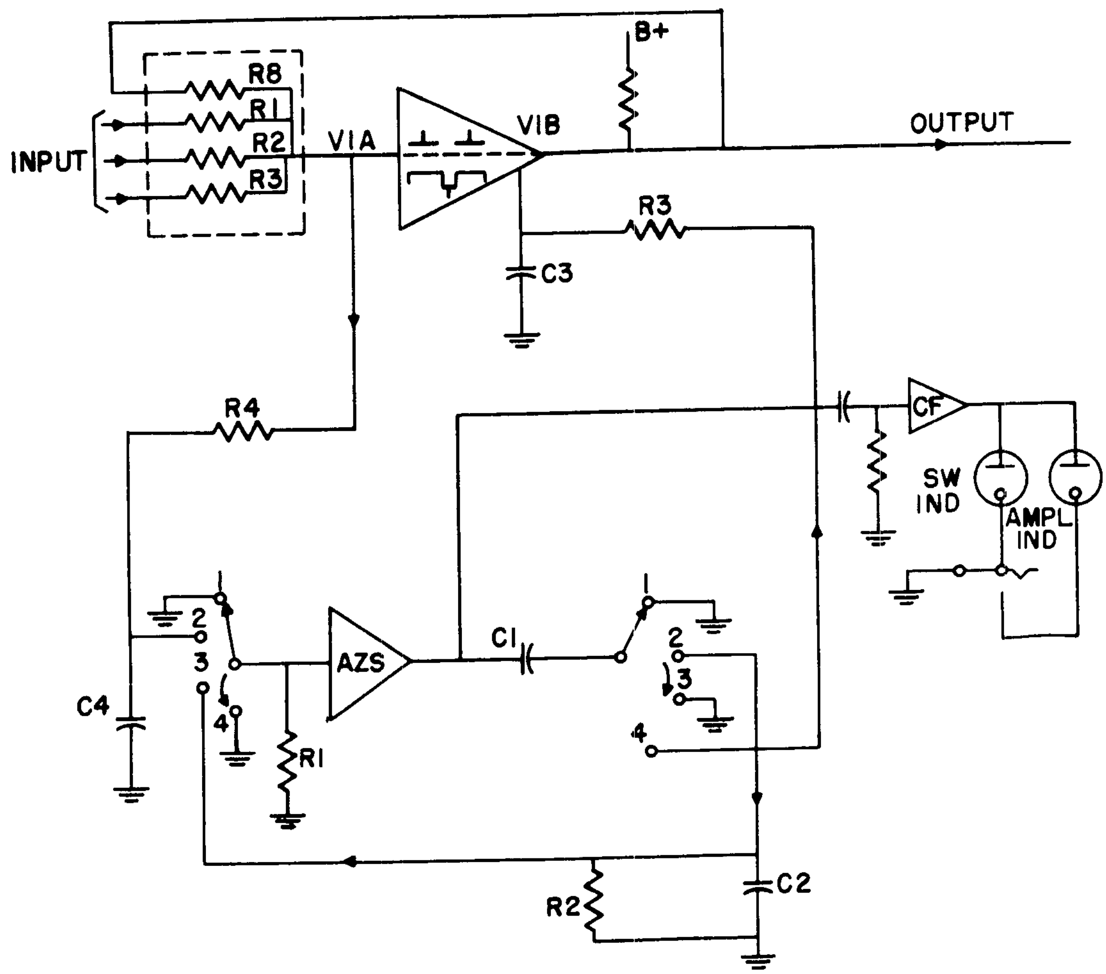

Figure 41. AZS syatem, precision reentrant type.

Section III. PRECISION ZERO SET SYSTEM

59. GENERAL (TM 9-5000-26)

The precision zero set system is used for zero setting the DC amplifiers in which more stringent requirements of computing accuracy are needed. Groups 1 and 5 (page 26C6) are precision zero set amplifiers. They are located at the top center of the equipment frames in the computer amplifier cabinets (page 29C5). The specifications for the precision automatic zero set system in the Nike I computer requires a voltage gain of 3,000 (70 db) in the AZS circuit. This gain is obtained through a circuit called the 4-step reentrant automatic

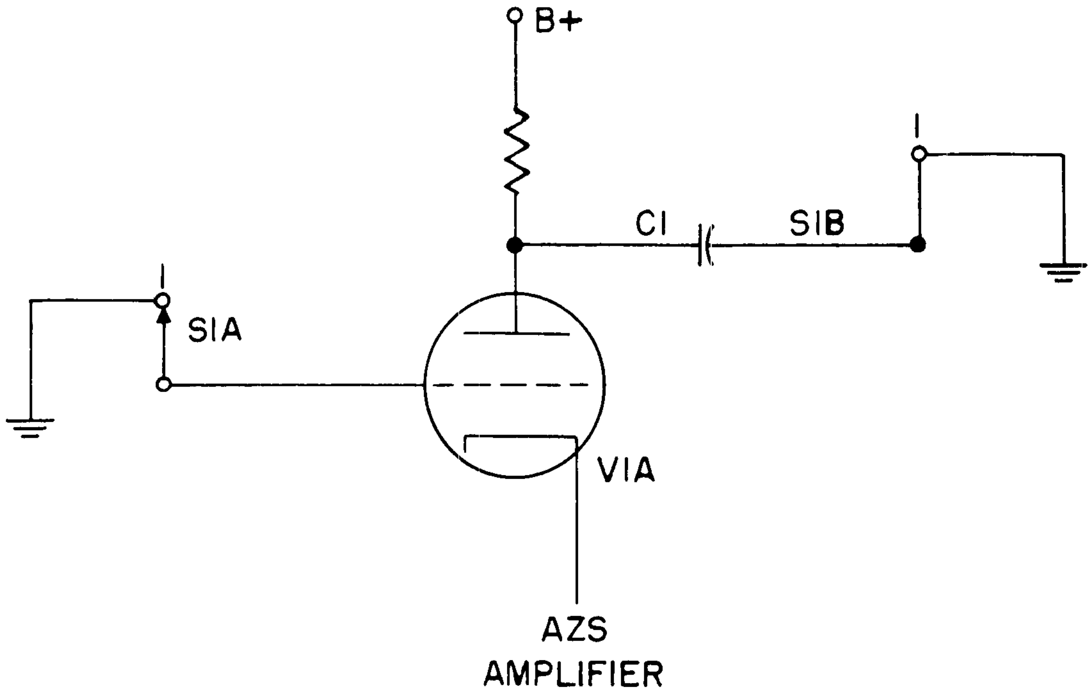

Figure 42. Step 1, precision reentrant AZS system.

zero set circuit. The same AZS amplifier and the same motor-driven rotary switch used in the semiprecision zero set systems are used. Each precision automatic zero set unit monitors only 6 DC amplifiers, since it takes 4 terminals for the 4 steps involved.

60. DETAILED FUNCTIONAL OPERATION (TM 9-5000-26)

The operation of the precision automatic zero set system is shown on page 26A1 to A5. This example shows the precision AZS system used in conjunction with the $+H_M$ amplifier. Although the DC amplifier is much more accurately zero set, the final outcome is the same; the error signal on the grid of V1A is made to approach zero. Even the method of zero setting is similar except for a few extra steps in the process. A simplified schematic of the reentrant method of automatic zero setting is illustrated in figure 41. This method requires four steps to zero set the DC amplifier. Assume that there is a positive error signal present on the grid of V1A. Capacitor C4 is charging to the magnitude of this positive voltage. In the first step of the reentrant system (fig 42), the grid of the AZS amplifier and the right plate of capacitor C1 are grounded. Capacitor C1 charges to the quiescent value of

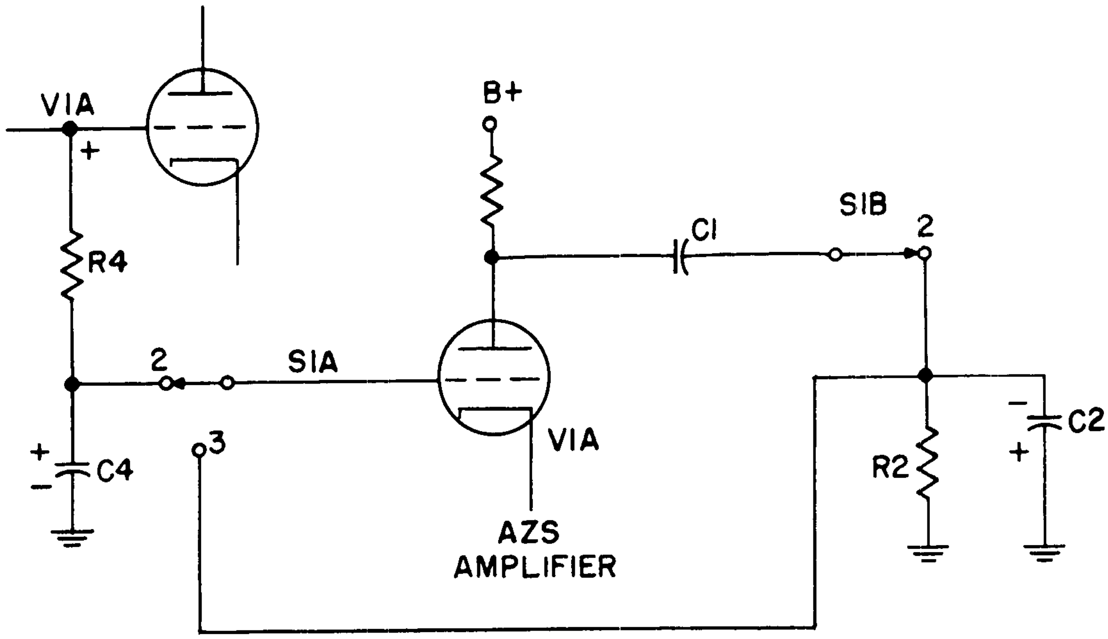

Figure 43. Step 2, precision reentrant AZS system.

the plate voltage of the AZS amplifier tube. This voltage depends on the value of the current through the tube; the charge on the cathode capacitor; and even on the prior values of the error signals on grid V1A of the DC amplifier. The important thing to remember is that C1 is now charged to a voltage which is used as a reference level. In the second step, the input to the AZS amplifier is connected to the junction of capacitor C4 and resistor R4, and the output is coupled through capacitor C1 to capacitor C2 and resistor R2 in parallel. Capacitor C4 is charged to the positive error voltage on the signal grid of V1A (fig 43) and is called the residual voltage. A positive signal on the grid of the AZS amplifier causes the plate voltage to go negative. This negative change is coupled through capacitor C1 and a fraction of it is stored on capacitor C2. Capacitor C1 remains essentially at the quiescent plate voltage. When the residual voltage is zero (no error signal on grid V1A), the voltage on C1 remains at the quiescent value of plate voltage, and the voltage on C2, having been zero, remains zero. In step three, the AZS amplifier is disconnected from the input of the DC amplifier, and the storage capacitor C2 is transferred to the input of the AZS amplifier. At the same time, C1 is grounded. The amplifier residual voltage on C2, a negative potential, is applied to the grid and amplified and reversed in polarity by the AZS amplifier. Capacitor C1 charges from the quiescent plate voltage to a voltage equal to the quiescent voltage plus the reamplified residual voltage. In the fourth step,

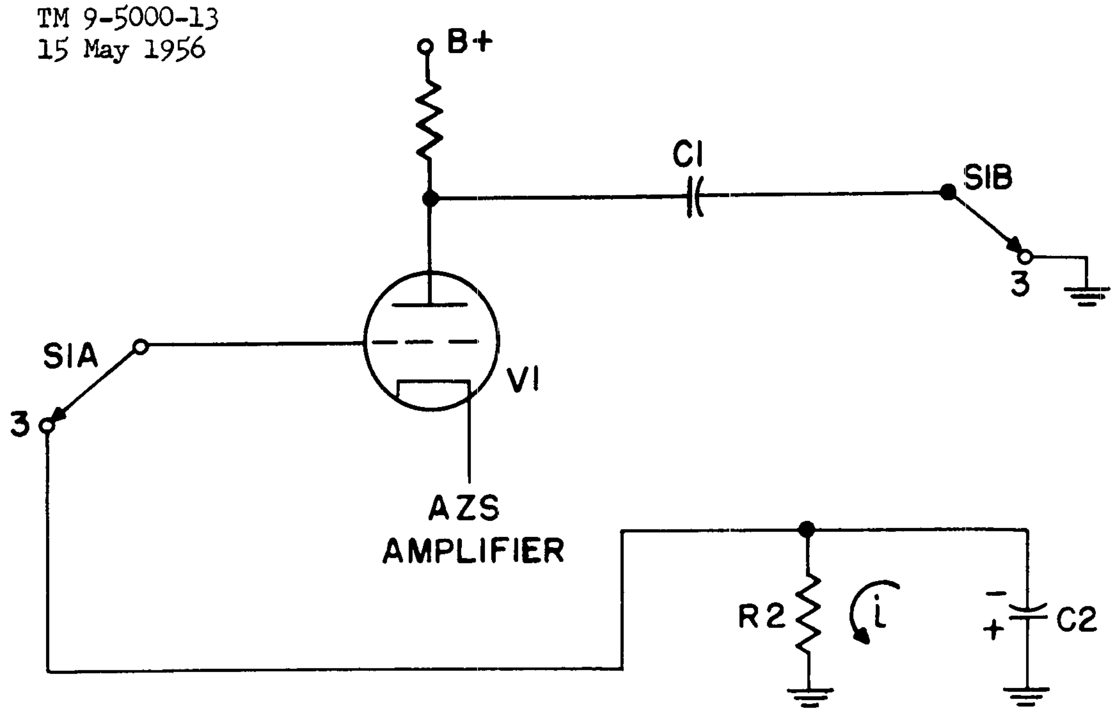

Figure 44. Step 3, precision reentrant AZS system.

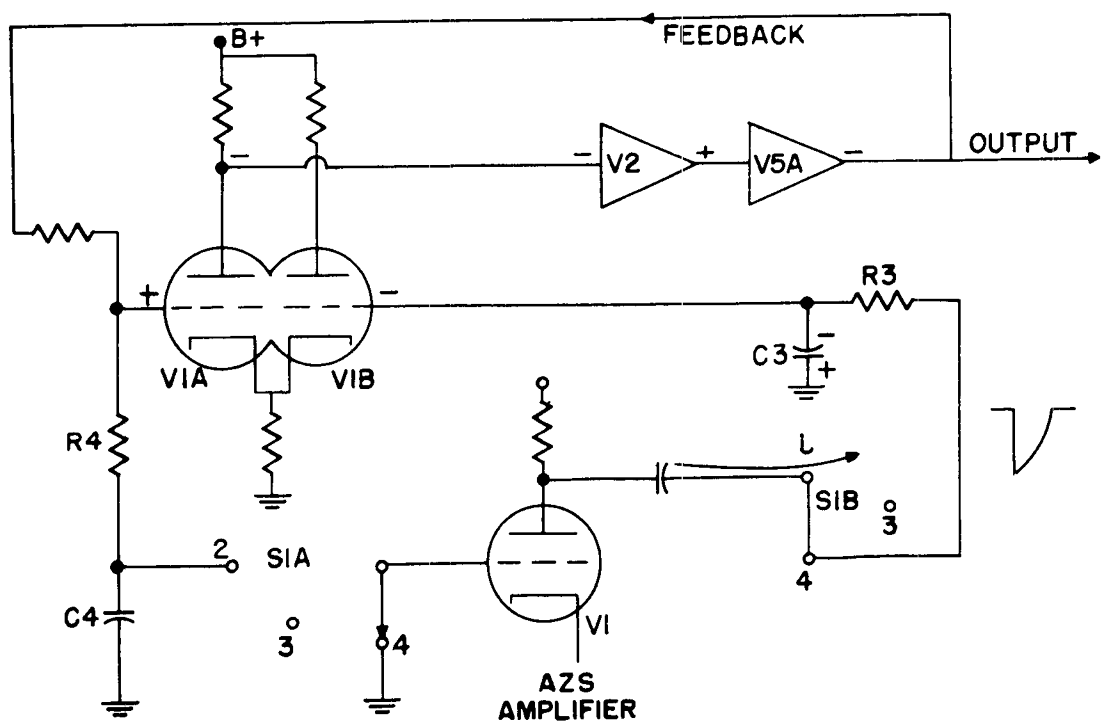

Figure 45. Step 4, precision reentrant AZS system.

the input to the AZS amplifier goes from a negative potential to ground, causing the grid to rise. At the same time, capacitor C1 is connected to the integrating circuit made up of capacitor C3 and resistor R3. The amplifier plate voltage goes negative returning to its quiescent value. The important thing is that the negative change in plate voltage is coupled through C1 and applied to the upper plate of capacitor C3. The values of C1, C3, and R3 are chosen so that C3 changes in voltage by an almost equal amount, but opposite in polarity to the error voltage on the grid of V1A. In figure 45, it can be seen that a positive error on the grid of V1A results in a negative voltage being applied to the grid of V1B. This is the correct polarity in voltage to make the positive error signal on V1A approach zero. In summary, a positive error on the signal grid, V1A, of the first stage of the DC amplifier is the result of an initial offset error, drift, or a mathematical error. Any or all of these voltages can reduce the feedback current, and cancellation of the voltage at the input grid, V1A, is not complete. Thereby, there is an error signal at the input of the DC amplifier when there should be zero voltage. If this positive error signal is sampled by the precision reentrant AZS system, a negative voltage is placed on the grid of V1B. The plate current through V1B is reduced, the common cathode becomes less positive, and plate current in V1A increases. The plate voltage of V1A drops and this negative change in voltage is amplified and reversed in V2, and amplified and reversed in V5A (fig 45). The output is a negative signal, part of which is fed back to the input grid of V1A to cancel out the positive error voltage. The precision AZS system is used with DC amplifiers that requires great accuracy to perform their functions properly. The gain of the precision system is 3,000 (70 db), which accounts for its extreme accuracy with respect to the semiprecision system whose gain is only 200. The magnitude of gain of the precision system will reduce the maximum expected voltage offset of 0.5 volts at the signal grid of the DC amplifier to approximately 0.13 millivolts.

61. MECHANICAL OPERATION

The precision AZS switch operates mechanically exactly the same as the semiprecision AZS switch does. However, the various pin connections are not the same. The GS-15557 switch used for the precision zero set system is shown in 2y, page 28. Using this rotary switch having 24 input and 24 output contacts, 6 DC amplifiers can be set by the 4-step reentrant system. In paragraph 58 a description of the mechanical operation of the AZS switch is given.

Section IV. OVERLOAD INDICATOR

62. GENERAL (TM 9-5000-26)

The use of the precision and semiprecision automatic zero set circuits requires that an indicator circuit be provided which will detect an overloaded DC amplifier. A cathode follower circuit (page 29) conducts enough on receiving an overload signal to give an indication by lighting a flashing neon lamp.

63. DETAILED FUNCTIONAL OPERATION (TM 9-5000-26)

The cathode follower circuit (page 29) consists essentially of a 2C51 tube, a twin triode, the two halves of which are operated in parallel. The cathode is biased at approximately zero potential and is capable of swinging a minimum of ±100 volts. Resistor R9 in the grid circuit of the cathode follower is large enough to prevent undue loading of the plate of the AZS amplifier tube. The 1μfd capacitor, C5, between the plate of the 6AK5 and the grid of the 2C51 is large enough to prevent appreciable alteration of its charge during the interval that a signal is applied to the AZS amplifier and, therefore, will cause no crosstalk. Resistors R7 and R8 prevent C5 from charging if the 2C51 draws grid current at any time. Resistors R11 and R12 act as a voltage divider to bias the grid at a value that keeps the voltage of the 2C51 approximately zero with no signal applied. When the cathode of the 2C51 is driven ±100 volts, the neon lamp will fire and enough current will be supplied to cause a bright flash. Two neon lamps are associated with each AZS unit for indicating a bad amplifier. One of the neon lamps is located on the computer control panel, and it indicates the AZS switch with the over-loaded DC amplifier. A second neon lamp is provided in the AZS switch. If the neon lamp at the computer control panel flashes, the computer operator goes to the indicated AZS switch and presses a nonlocking key on the switch, which transfers the indication to the neon lamp in the AZS switch. Through a lucite arm that rotates with the shaft of the switch and numbered holes in the cover, the overloaded or bad amplifier on the AZS switch can be identified. A permanently lighted neon lamp indicates the failure of the cathode follower tube. There is no permanent indication for the failure of the 6AK5 tube.

amplitude of 60 volts. The two voltages are 180° out of phase. From figure 46, it is apparent that these two voltages are each 90° out of phase with phase C (mtr X).