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Computer Development (SEAC and DYSEAC) at the National Bureau of Standards Washington, D. C.

UNITED STATES DEPARTMENT OF COMMERCE

NATIONAL BUREAU OF STANDARDS

UNITED STATES DEPARTMENT OF COMMERCE • Sinclair Weeks, *Secretary*
NATIONAL BUREAU OF STANDARDS • A. V. Astin, *Director*

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Foreword

Since 1946 the National Bureau of Standards has been active in the general field of electronic digital computers, largely for other agencies of the Government. The Bureau's computer program has been conducted jointly by the Electronics Division and the Applied Mathematics Division. The work of the Electronics Division in Washington has included the development and construction of two computers (SEAC and DYSEAC), components research and development, and various technical and advisory services. The work of the Applied Mathematics Division has included research in numerical analysis of importance in the solution of problems by computers and the design and construction of a computer (SWAC) at the Bureau's Institute for Numerical Analysis in Los Angeles.

This volume presents reports on various aspects of the computer program through 1953, based largely on the work and experience relating to SEAC and DYSEAC. Such topics as systems development, engineering development, design, construction, and maintenance of computer equipment are covered. The introduction summarizes the history of this program in the Electronic Computers Laboratory of the Electronics Division.

A. V. Astin, *Director.*

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Introduction

S. N. Alexander

The development of electronic digital computing machinery at the National Bureau of Standards started in 1946 because of the interest of the Bureau of the Census in the possible use of electronic digital techniques for tabulating purposes. In particular, the Bureau of the Census hoped to attain trial use of an electronic installation in connection with the 1950 decennial census, and the National Bureau of Standards was asked to provide technical guidance and developmental support to this long-range program. Concurrently, NBS was seeking to obtain an electronic digital computer as a scientific instrument for its own use. Immediately following the establishment of these two tasks, a 2-year program for the development of improved components for digital computers was established under the sponsorship of the Office of the Chief of Ordnance, Department of the Army.

The relatively short time schedule desired for the delivery of the two complete machine installations, together with suitable auxiliaries and operational supplies, made it advisable from the outset to seek commercial sources for such equipment. In this way, it seemed possible to compress the research, development, and construction of such equipment into an integrated effort and thereby meet the time schedules. This decision was buttressed by further requirements from the Office of Air Comptroller, Department of the Air Force, and the Army Map Service for similar equipment with comparably short time schedules. NBS agreed to serve as technical agent in monitoring the design, construction, and installation of these machines from two commercial suppliers, while its own laboratories were fully occupied with the component development program.

Because of an unanticipated sequence of technological and contractual difficulties, it became evident early in 1948 that the delivery of complete machine installations would be delayed considerably beyond the target dates. The unexpected difficulties associated with the developmental phases of all such programs, both commercial and university, emphasized the uncertainty of availability of electronic digital computing facilities of any sort. This motivated a request for a "stopgap" installation to serve some of the urgent needs of both the Air Comptroller and NBS during the interim period until full-scale equipment could be obtained from commercial sources within a more realistic time schedule. During the summer of 1948, NBS explored the possibilities of designing and constructing an interim machine that would have sufficient power for general use and yet be simple enough to be constructed in a short time. The feasibility of this program was based on the preceding 2 years of active experience in component development and the availability of the best technology that had been reported by other computer groups, particularly those in the universities.

The original modest objectives for an interim machine were reconsidered toward the end of 1949, when it became evident that the proposed SEAC computer would be the only equipment available to NBS and collaborating Government agencies for at least 2 years. To cope with this altered situation, the plan for the machine was adjusted so that a full-scale installation could be attained by subsequent expansion of an initial nucleus. However, the prime objective was still to have the initial nucleus in operation at the earliest possible date. The resulting machine began useful operation in May 1950, less than 2 years after the start of the program, and SEAC completed nearly a year of scheduled operation for NBS and its collaborators before any other installation was available to them. Furthermore, SEAC was the one installation that was readily available to serve the intermittent computational needs of many other Government agencies, and for over 2 years was used on a round-the-clock basis for the full 7-day week. Even now, after 3 years of regularly scheduled operation, the SEAC is still employed for an extended work week in the solution of problems.

The task of designing a large-scale digital computer such as SEAC from original conception to final realization was, of course, the effort of many minds and the work of many hands. The team chosen for this task encompassed a wide spectrum of talents and skills. The successful completion of SEAC at a time when the availability of such a facility was of urgent importance to the Government was recognized by the Award for Exceptional Service from the Department of Commerce to the

SEAC staff as a group. In addition to this group-citation to the 33 scientists and technicians who contributed to the SEAC accomplishment, particular mention was made of the individual contributions by S. N. Alexander, W. W. Davis, R. D. Elbourn, S. Greenwald, R. C. Haueter, A. L. Leiner, S. Lubkin, C. H. Page, J. L. Pike, R. J. Slutz, and J. R. Sorrells. The early contributions of H. Senf and W. Martin also deserve recognition, even though they did not remain to participate in the completion of SEAC.

As soon as the central nucleus of SEAC was functioning reliably enough to warrant regularly scheduled operations, the program of expansion and additions began. Indeed, the machine became a proving ground for the evolution of advances in computer components, design techniques, and maintenance procedures. The expansion and testing were carried out in the midst of a regular work load of important computing that was tightly scheduled because of priorities. Thus it was necessary to plan carefully in order to meet the requirements for scheduled computation and also include the necessary development work. The fact that these two conflicting objectives were meshed in an effective manner is a compliment to the fine cooperation and management between the scientists and engineers who designed SEAC and the mathematicians who used it.

During this period of expansion, over 90 percent of the time available in a full 168-hour week was effectively scheduled and used for either problem solution, development work, or preventive maintenance. During this period, 83 hours a week were scheduled for problem solution, of which 65 percent was logged as productive time, and 52 hours a week were scheduled for development work. Only 20 percent of the time scheduled for either development work or problem solution was recorded as being ineffective because of machine malfunctions. This is considered a gratifying performance for a pioneering installation, particularly when the difficult tasks of operating and expanding the machine were under way at the same time.

The initial program for expansion was directed primarily at the task of improving the input-output facilities, which resulted in the addition of magnetic wire and magnetic tape units to increase the speed of computation on problems that could not readily be kept within the confines of the 512 words available in the high-speed memory. As more of these magnetic units became available, an external selector panel was added to the machine to permit automatic selection of the desired input-output unit under programmed control of the computer as well as by manual operation of the console switches. This, in turn, made it necessary to design and construct both an inscriber and an outscriber to facilitate the transition between the documents containing the coded problem and the typed sheets giving the results of the computation by the machine. In addition, arrangements were made to permit transfers to and from punched cards which were either the source for data or the final form desired for the solution. Most of the effort in this area was planned and directed by R. J. Slutz, with the able collaboration of S. Greenwald, R. C. Haueter, E. F. Ainsworth, J. L. Pike, L. Cahn, P. R. Westlake, W. H. Bridge, and P. D. Shupe, Jr.

While the input-output system of SEAC was being augmented, steady planning and construction by a group under the leadership of W. W. Davis were also under way for the addition of an experimental electrostatic memory, primarily for trial and evaluation but with the eventual goal of regular service as an additional 512-word high-speed memory. This equipment also served as an exacting evaluation of experimental cathode-ray tubes specifically designed for storage purposes and of testing procedures that were being developed for selecting tubes suitable for operation in the memory.

The central control of the machine also underwent considerable revision and expansion. Some of these changes related to the inclusion of additional machine operations, but the more significant changes related to the inclusion of an automonitor function and a three-address control system, which is described in detail in one of the following papers. These revisions and expansions resulted from suggestions arising out of operational experience and the desire to make the machine more versatile. The detailed planning of these changes was the work of A. L. Leiner, who had been responsible for most of the final system plans for the SEAC nucleus. The physical realization and installation of these new features are a tribute to a combination of careful engineering and patience on the part of R. C. Haueter, S. Greenwald, and P. D. Shupe.

Sporadic performance of the experimental electrostatic memory directed specific attention to the development of an improved cathode-ray tube for storage purposes. By this time, the Bureau had begun the planning of a far more powerful machine than SEAC to be used in the SCOOP program of the

Office of Air Comptroller. This machine definitely required a rapid-access memory, and for this reason the development of both cathode-ray tubes and improved electrostatic storage techniques was pursued vigorously, under A. W. Holt and D. C. Friedman. Meanwhile, other approaches to rapid-access storage were being explored, one of which resulted in the Diode-Capacitor memory system suggested by A. W. Holt and reported in a companion paper.

During the expansion of SEAC and the evaluation of components aimed toward the creation of a SCOOP machine, it became evident that the dynamic circuitry devised for SEAC was susceptible to considerable electronic standardization. In turn, this became the basis for a repetitive physical configuration out of which the high-level pulse circuitry could be assembled. The advantages and possibilities of a standardized package design were realized by R. J. Slutz, and its detailed design and execution were the results of combined efforts of R. P. Witt and R. D. Elbourn.

The computer group at the U. S. Air Force Missile Test Center, Patrick Air Force Base, Cocoa, Florida, collaborated in the mechanical design of the first satisfactory packages, and these were successfully employed in the outscriber that was constructed for SEAC. This packaged design, with some refinements, was used in two computing machines that have recently been completed, one at the Air Force Missile Test Center and the other at the Willow Run Research Center of the University of Michigan. The Bureau revised this package design to incorporate etched circuit techniques. These are the packages that were used in the construction of DYSEAC, a new machine sponsored by the Research and Development Board for the evaluation of a number of organizational and engineering innovations. All three of these machines are based on the circuit techniques and some of the organizational features of SEAC, but they are distinguished one from the other by variations on the SEAC organization that were included to meet specific application requirements.

In order to cover adequately the 5 years of development that stemmed from the SEAC program, the component improvement program, and the subsequent DYSEAC program, the senior personnel of this laboratory have shared the responsibility for reporting on the achievements of the entire group. The authors of any of these particular papers are not necessarily, therefore, the only major contributors to the solution of problems discussed; and many of these authors, with others, have made important contributions to other programs as well as to those on which they are now reporting. Here again, it is important to recognize the team nature of the developmental activity that is being carried on at NBS.

While the detailed planning of the SCOOP computer was deferred in order to identify more clearly its operating characteristics and to have at hand a proved rapid-access memory, the design and constrution of DYSEAC, which was to result in a complete machine that would serve certain specialized needs and also provide a thorough evaluation of the packaging techniques, was undertaken. Although DYSEAC employs an acoustic memory and a serial arithmetic unit, the basic organization is considerably more sophisticated than that of SEAC, for it contains some of the system features that had been planned for the SCOOP machine. In addition, special features have been incorporated to permit the machine to serve as a tool for experimentation on the handling of large masses of business-type data and for experimentation in using digital equipment in a control system.

The task of planning the organization of DYSEAC and its detailed execution through the preparation of wiring tables was carried out under the direction of A. L. Leiner, with the able collaboration of W. A. Notz, J. L. Smith, A. Weinberger, and W. H. Bridge. The physical realization of the machine involved many original design problems related to the use of packages and a modular type of construction for the chassis. The decision to install DYSEAC in a pair of vans was made after the program was well under way. This added many new mechanical and electrical considerations. The formidable task of constructing DYSEAC was accomplished in approximately 18 months by a team of about 25 people directed by R. P. Witt, ably supported by R. W. Smith, H. P. Belcher, and R. Hand.

One of the major purposes in the SEAC program was to evaluate the reliability and serviceability of techniques that appeared highly promising but were at that time still unproved. Subsequent operating experience has established the soundness of many of the engineering choices that were significant departures from the techniques then current. Operating experience established another important feature: the significant benefits that accrued from using an operating machine as a proving ground for new component and operating techniques. SEAC has served as a valuable focal point that prompted the exchange of ideas among the components researcher, the machine designer, the maintenance engineer, and the user. The DYSEAC holds promise of becoming a comparable source of ideas for further machine development.

1. SEAC

S. Greenwald, S. N. Alexander, and Ruth C. Haueter

1. INTRODUCTION

The first major contribution of the National Bureau of Standards to the development of electronic computing machinery occurred with the completion of the SEAC (Standards Eastern Automatic Computer) in May 1950. This digital machine was the culmination of almost 2 years of intensive design and construction work which was sponsored by the Office of Air Comptroller, Department of the Air Force. The initial objective set during the summer of 1948 was to provide at the earliest possible date a machine of limited computing power that would meet the immediate computational needs of the National Bureau of Standards. This installation would serve as a "stopgap" for the interim period during which full-scale equipment from a commercial source was being completed for delivery to the Government. Toward the end of 1949 this point of view was gradually abandoned, as it became evident that there would be no other equipment available for 2 years or possibly longer. As a result, the ultimate objective was altered so that a full-scale machine could be attained by expansion of the initial nucleus without delaying its completion.

Still another aspect of building an expandable machine was the ability to use it as a proving ground for experimental equipment.

At the present time, after more than 3 years of regularly scheduled operation, SEAC is still actively employed in the solution of problems for both NBS and many Government agencies. What is perhaps more important is that for the initial 2 years of its operation it was the most powerful computer installation readily available to the Government, and consequently was scheduled around-the-clock for a full 7-day week.

Since the machine was first put into operation, a significant fraction of the total time available has been devoted to the engineering work associated with the expansion of SEAC. The magnitude of this effort can be estimated from the fact that the number of vacuum tubes in the system was increased from approximately 750 to 1,300 and the number of germanium diodes from approximately 10,500 to 16,000. This expansion and testing program was carried out in the midst of a regular work load of important computation that was tightly scheduled because of priorities.

A number of circuit and equipment innovations were included in the SEAC program in order to evaluate the reliability and serviceability of techniques that were highly promising but unproved. One example in this area is the extensive use of diode switching. Another is the achieving of a-c coupling by using pulse transformers for highly variable duty factor service. Success with these techniques made practical the use of vacuum tubes as a means of power amplification rather than as gating devices.

At the present, two machines based on a packaged version of the SEAC "transformer-coupled dynamic circuitry" have been completed. One is located at the Air Force Missile Test Center in Florida and the other at the Willow Run Research Center of the University of Michigan. A still further extension of these techniques was employed at the National Bureau of Standards in the construction of the DYSEAC, which is described in a companion paper.

2. OPERATING CHARACTERISTICS

The SEAC is an automatic high-speed digital computer that operates at a 1-Mc pulse repetition rate. The machine is predominately serial in nature and uses the binary number representation. Both instruction words and number words consist of 45 binary digits, which are equivalent to approximately 13 decimal digits. When the machine was first put into operation in May 1950, 11 different types

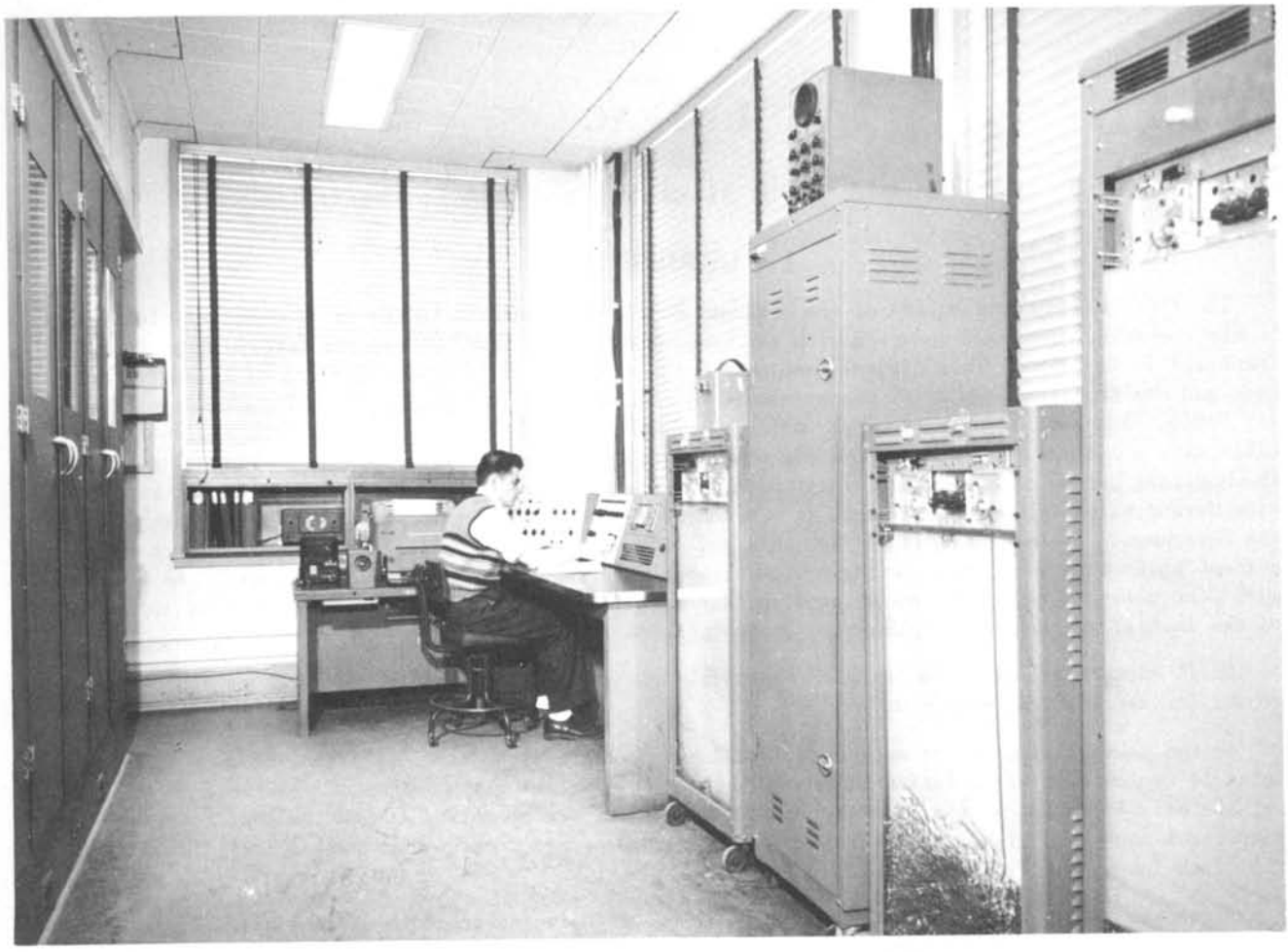

FIGURE 1.1. *SEAC from control console side.*

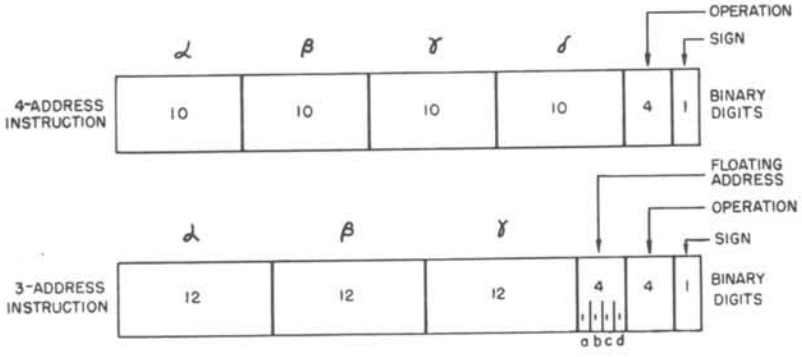

FIGURE 1.2. *Component parts of a SEAC instruction.*

of operations were performed by it: (1) addition, (2) subtraction, (3) multiplication, major part, unrounded, (4) multiplication, major part, rounded, (5) multiplication, minor part, (6) division, (7) comparison, algebraic value, (8) comparison, absolute value, (9) logical transfer, (10) read in, and (11) print out. The instruction words expressed these operations in the four-address mode. The original high-speed memory consisted of 512 words of acoustic delay-line storage, and all of the input-output devices were modified Teletype equipment. The input was from either a tape reader or keyboard, and the output was to either a printer or tape punch.

During the 3 years the machine has been operating, it has been expanded into a far more powerful and convenient tool than its original conception. For example, five additional operations have been incorporated: (1) reverse tape or wire, (2) logical multiplication, (3) base, (4) file counter information, and (5) clear memory cell, bringing to a total of 16 the types of operations available. An experimental Williams type of electrostatic memory has also been added. This stores 512 words in 45 cathode-ray tubes, with parallel access to a complete word in 12 μsec. An alternative instruction system, using the three-address mode of operation has also been installed. By simply setting several switches inside the machine, the computer is set for operation in either the three-address or four-address system.

Magnetic wire and magnetic tape units were added to increase the speed of the computer on problems which require considerable input-output or auxiliary memory capacity. In particular, the magnetic wire handling equipments greatly speed up initial input and final output. Magnetic tape units, both single-and multiple-channel, provide external memory. Figure 1.1, which is a view of the computer from the console side, shows several of these units. Either automatic or manual selection of input-output units is available. Still another feature that has been added by modification of the circuitry is the ability to automatically monitor the operations being performed. When called into use by setting a switch on the console, this feature causes the machine to print out the program-sequence counter information, the instruction being performed, and the result of the operation. This facility is a great convenience, and will be discussed in more detail later.

The component parts of an instruction word in both the four-address and three-address systems are shown in figure 1.2. In the four-address system, the addresses are denoted by the symbols α, β, γ, and δ. Normally, α is the address of the first operand, β the address of the second operand, γ the address of the result of the operation, and δ the address of the next instruction. The instruction also contains a code specifying the type of operation to be performed and a conditional halt control digit in the sign position. An address comprises 10 binary digits, so it can designate one out of 2^{10}, or 1,024, memory cells. This is sufficient for the two SEAC memories. Four binary digits specify the operation to be performed. The 16 different operation codes thus available are now all used. The single binary digit in the sign position indicates whether or not the computer is to halt after performing the operation. In the course of executing one instruction, the control of the computer cycles through four phases, one for each reference to the memory. In a typical operation, address β is referred to in phase 2, α in phase 3, γ in phase 4, and δ in phase 1.

A typical three-address instruction word contains the addresses α and β of the operands and the address γ of the result. The remainder of the word contains floating-address information, the code specifying the type of operation to be performed, and the conditional halt digit. Twelve binary digits are used to specify an address, providing the basis for selection among 4,096 memory cells; four binary digits are used to provide information for the floating address feature. The operation code for the 16 instructions is the same as in the four-address system.

The main difference between the three-and four-address systems is in the designation of the next instruction to be performed. In the four-address system, the instruction contains an explicit statement (δ) designating where the next instruction is located in the memory. In the three-address system, however, there is no such explicit statement. Instead, instructions in this system are automatically sequenced in accordance with a convention, successive instructions being normally located in consecutively numbered memory positions. An exception to this convention is available through the comparison (conditional transfer) operation, whenever the first operand (α) is less than the second operand (β). In this case the result of the comparison leads to what is called a "jump" operation in which the next instruction for both the three-address and four-address systems is chosen from address γ.

The floating address feature allows the programmer to designate any address as either absolute or relative. An absolute address is interpreted in the usual sense, merely as a number identifying a specific memory location. A relative address, however, identifies a position in the memory by specifying its displacement relative to that position from which the instruction word itself was taken. To illustrate, suppose that an instruction located in memory position m specifies that the address of the first operand is number 17 relative. Then the control will take the word in memory location $(m+17)$ and use it as the first operand. If location $(m-17)$ is desired, the complement of 17 is used as the address.

It is possible to use any combination of absolute or relative addresses in an instruction word. Of the four binary digits that supply floating address information, the first three digits, a, b, and c, indicate whether α, β, and γ, respectively, are absolute or relative. The fourth binary digit d tells which of two control counters is to be used during operation in the three-address mode. Counter 0 is normally the operating counter. However, starting with any desired address, counter 1 can be put into operation by a "jump" comparison in which γ is the desired address and binary digit d specifies counter 1. Counter 1 will be the operating counter only so long as d in each following instruction indicates counter 1. As soon as an instruction is reached in which d indicates counter 0, the control automatically returns to counter 0 after performing the instruction.

A typical use of this feature is to code subroutines for counter 1 with floating addresses. The use of floating addresses allows the subroutine to be placed anywhere in the memory automatically. By coding a subroutine for counter 1, a "jump" comparison sends the control to counter 1 at the desired address, and after finishing the subroutine it returns the control automatically to counter 0 at the point in the main program where it left off.

The basic operations of SEAC and their functions are summarized in table 1.

TABLE 1

Name of operation	Description of instruction
Addition	Form the sum of the word in α and the word in β, and write the result in address γ in the memory.
Subtraction	Form the difference α minus β, and write the result in address γ in the memory.
Multiplication, major, unrounded.	Form the product of the word in α and the word in β, and write the major part (unrounded) in address γ in the memory.
Multiplication, major, rounded.	Form the product of the word in α and the word in β, and write the major part (rounded off) in address γ in the memory.
Multiplication, minor	Form the product of the word in α and the word in β, and write the minor part in address γ in the memory.
Division	Form the quotient of the word in β divided by the word in α, and write it in address γ in the memory.
Logical transfer	Write in address γ in the memory those digits of the word in α which correspond to one-digits of the word in β. Leave the word in γ unchanged in those digit positions which correspond to zero-digits in the word in β.
Comparison, algebraic	If the word in α is algebraically greater than or equal to the word in β, take the next instruction from the normal next-instruction address position. (In the four-address system, this is address δ in the memory; in the three-address system, this is the next consecutively numbered address position.) If, however, the word in α is less than the word in β, take the next instruction from address γ in the memory.
Comparison, absolute	Perform algebraic comparison except treat both words as positive.
Read in	If the address number β is odd, read in one word from the selected external unit designated by address number α, and write the data in address γ in the memory; if the address number β is even, read in eight words, and write in the eight addresses beginning with address γ.
Print out	Print out the word in address γ in the memory if the address number β is odd (or the block of eight words beginning with address γ if β is even) onto the selected external unit designated by address number α.

TABLE 1—Continued

Name of operation	Description of instruction
Reverse	Reverse through one word if the address number β is odd (or through eight words if the address number β is even) on the selected external unit designated by address number α.
Logical multiplication	Write the digit-by-digit product of the words in addresses α and β into address γ in the memory.
Base (primarily for four-address system).	If address number α is greater than or equal to address number β, put the number β into the special base-number counter-register and take the next instruction from address δ in the memory. In subsequent instructions, all references to odd-numbered addresses will now be interpreted relative to this constant number β. If address number α is less than address number β, the counter-register is cleared and the next instruction is taken from address γ in the memory.
File	Write the contents of special counter-registers into memory address γ.
Clear	Clear memory address γ.

3. MACHINE ORGANS

An over-all block diagram of SEAC is shown in figure 1.3, in which information paths are shown as solid lines and control paths as dashed lines. Interchanges of information between the Shift Register, the Arithmetic Unit, the Control, and the Mercury Memory are made through the unit called the Bus. The Bus not only provides correct routing of information but correct timing as well. During an input operation, instructions and numbers are read into the Shift Register from one of the input-output units via the Selection Circuits. From the Shift Register there are two possible paths. The digits are transferred either in parallel into the Electrostatic Memory or serially into the Mercury Memory via the Bus. For an output operation, the procedure is the same but the path is reversed. For internal operations, instructions are routed from the Memory to the Control Unit, and numbers are routed between the Memory and the Arithmetic Unit. Transfers are made to and from the Mercury Memory directly through the Bus. Whenever the Electrostatic Memory is used, an additional transfer through the Shift Register is required.

The Arithmetic Unit in SEAC is involved in almost every operation that the computer performs, with the exception of several such as File and Base. Figure 1.4 is a block diagram of the Arithmetic Unit. In the process by which two numbers are added, the first number enters the Arithmetic Unit in phase 2 of the cycle through which the computer sequentially progresses. If the number is positive, it goes through the Input Complementer and Adder into the Accumulator Register. If the number is negative, the Sign Sensing Unit activates the Input Complementer, and the complement of the number is sent to the Accumulator Register. During phase 3, the second number is sent to the Arithmetic Unit. Again it is complemented or not, depending on whether it is negative or positive. The second number is then added to the first number, which has been circulating in the Accumulator Register and is available at the second input to the Adder. In phase 4, the result of the addition is sent via the Output Complementer through the Bus connection to the Memory. If the result is negative, the Sign Determining Unit inserts a binary 1 in the sign position of the number and also activates the Output Complementer.

The process of subtraction is almost identical, the difference being that the effect of the sign of the number from β on the Sign Sensing Unit is reversed. The process for a comparison is similar to that for subtraction. However, no result is transferred to the memory; instead a signal is sent to the Control Unit when α is less than β.

Multiplication is performed in SEAC by repetitive additions, which involve the use of two other registers, the Multiplier and the Multiplicand Registers. In phase 2, β enters the Multiplier Register, and in phase 3, α enters the Multiplicand Register. Multiplication is accomplished by successive additions of the multiplicand to the partial product in the Accumulator Register under the control of the digits of the multiplier. The shifting is accomplished in the Accumulator Register by shortening it one pulse time. Division is also a repetitive process using all three registers,

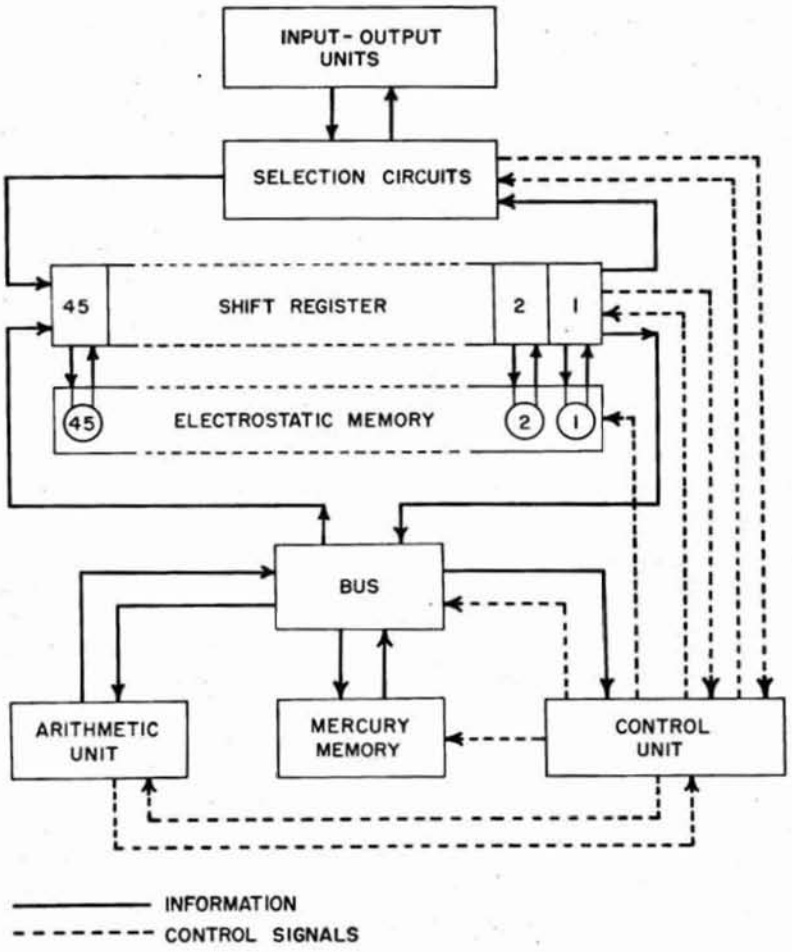

FIGURE 1.3. *Block diagram of SEAC.*

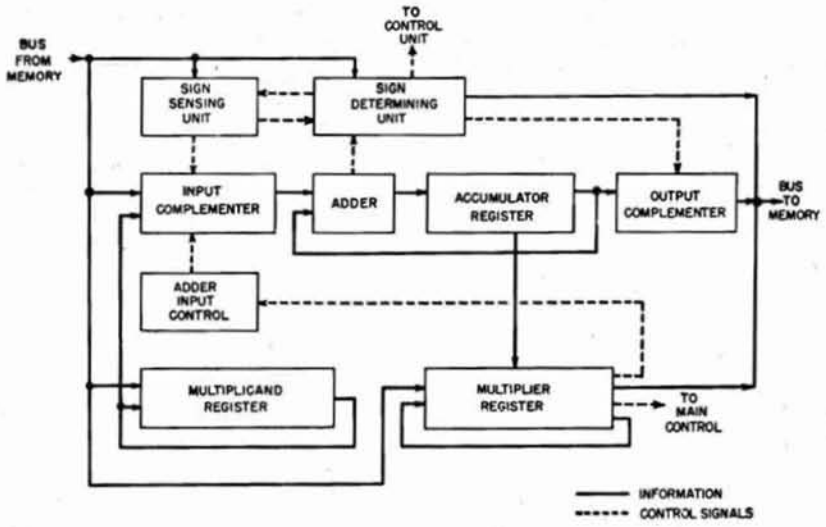

FIGURE 1.4. *Block diagram of Arithmetic Unit.*

with the quotient formed in the Multiplier Register. The nonrestoring method of division is used and consists of successive subtractions or additions of the divisor, according to the sign of the remainder. Physically, the entire Arithmetic Unit occupies only 1 1/4 relay racks. It is interesting to note that this early design for a binary adder, which is used in all computations, employs only three single-cathode vacuum tubes.

The Control Unit is the most complex part of the computer, as may be seen in the simplified block diagram of the control in figure 1.5. This has resulted partially from the experimental nature of the machine and from the continuous expansion it has undergone. One of the major functions of the Control Unit is to decode the instruction to determine (1) the type of operation to be performed, (2) the location of the numbers involved in the operation, and (3) the location of the instruction to be performed next. After the instruction is received from the memory, it circulates in the Instruction Register. The digits representing the operation are decoded in the Staticizer and Decoder, and the appropriate operation lines are activated.

The addresses are selected one at a time in what is called the Address Selector. If the location called for is in the Mercury Memory, the address information is sent to the Mercury Comparator. When the output of the Minor Cycle Counter agrees with the temporal selection portion of the address, the Mercury Comparator sends a signal to the Execute Generator that the desired word is in position to be read out. The Phase Counter is then advanced and the transfer is made. On the other hand, if the location called for is within the 512 words of the Electrostatic Memory, the address is routed into the Electrostatic Control. This Control then determines when the Execute Generator will advance the Phase Counter and when transfer between the Electrostatic Memory and the Shift Register will be made. In three-address operation the information from the selected counter is sent to the Address Selector where it is used to select relative addresses and the location of the next instruction.

The Shift Register Control serves mainly to direct the transfer of information in and out of the Shift Register at the rate acceptable to the Input-Output device in use. The Automonitor Control automatically cycles the computer through the necessary print-outs for each instruction being monitored. The Multiplication Counter counts off the 44 minor cycles (word times) necessary for a multiplication or division and prevents the phase counter from advancing until this portion of the operation is completed. Finally, the Manual Control permits the computer to be started or stopped, or its operation to be modified, by means of switches located on the console.

The Mercury Memory for SEAC is housed in a separate cabinet, which contains the 64 mercury-filled acoustic lines, their associated amplifiers and gating circuits, the selection matrix, and other miscellaneous circuitry. Figure 1.6 shows one side of the cabinet with 32 of the recirculation amplifiers and half of the selection circuitry. As the nominal delay through the lines is 384 μsec, 8 words of 48 digits each are stored in each mercury line. Thus the total capacity of the memory is 512 words.

Because the delay of a mercury line varies somewhat with temperature and yet the whole memory must be kept in step with the crystal-controlled computer clock, it is necessary to maintain all lines at the same constant temperature. A system of aluminum plates and extrusions bonds the 64 mercury-filled glass tubes into a nearly isothermal unit, which is insulated from the outside and is electrically heated and thermostated to 50 $\pm 0.25^{\circ}$ C.

Pulses are stored in each line as packets of an 8-Mc carrier. For every binary one there is an associated radio-frequency pulse packet, and for every zero there is a gap. The acoustic output of the line activates a quartz crystal whose electrical output is then transformer-coupled to the input of the recirculation amplifier. The first three tubes serve as a radio-frequency amplifier and detector, with an over-all gain of 50 to 55 db and a center frequency of 8 Mc. The fourth tube in the chain has the function of switching information into or out of the line, as well as that of synchronizing and reshaping. The fifth tube develops the 8-Mc packet of 200-v peak-to-peak amplitude, which is transformer-coupled to the input crystal of the mercury line.

Figure 1.7 shows the general organization of the mercury cabinet. Digital information denoting the mercury line to be selected comes from the Mercury Comparator located in the control section of the machine. An electrical delay line brings these time sequential pulses into positions from which

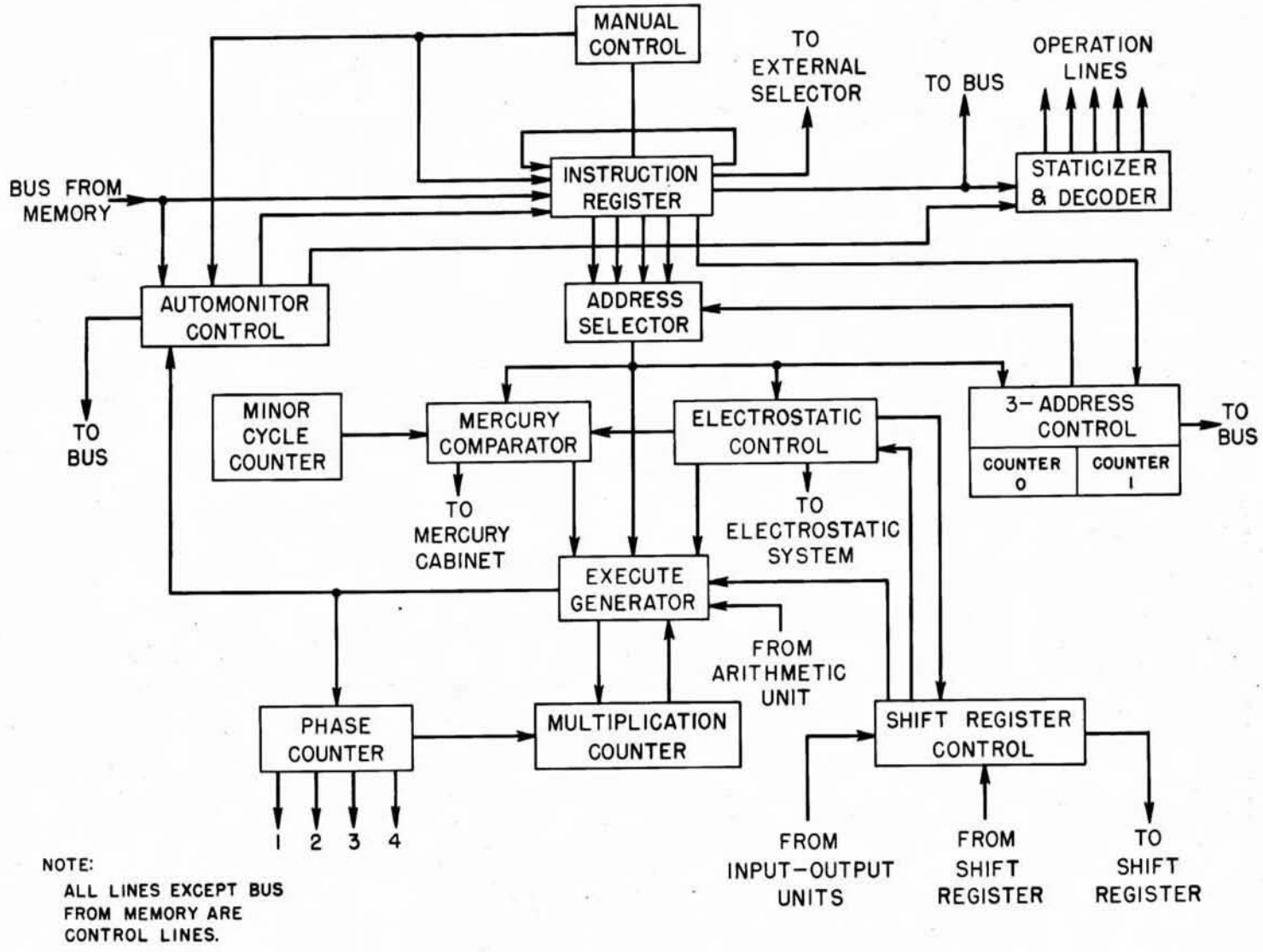

FIGURE 1.5. *Block diagram of Control Unit.*

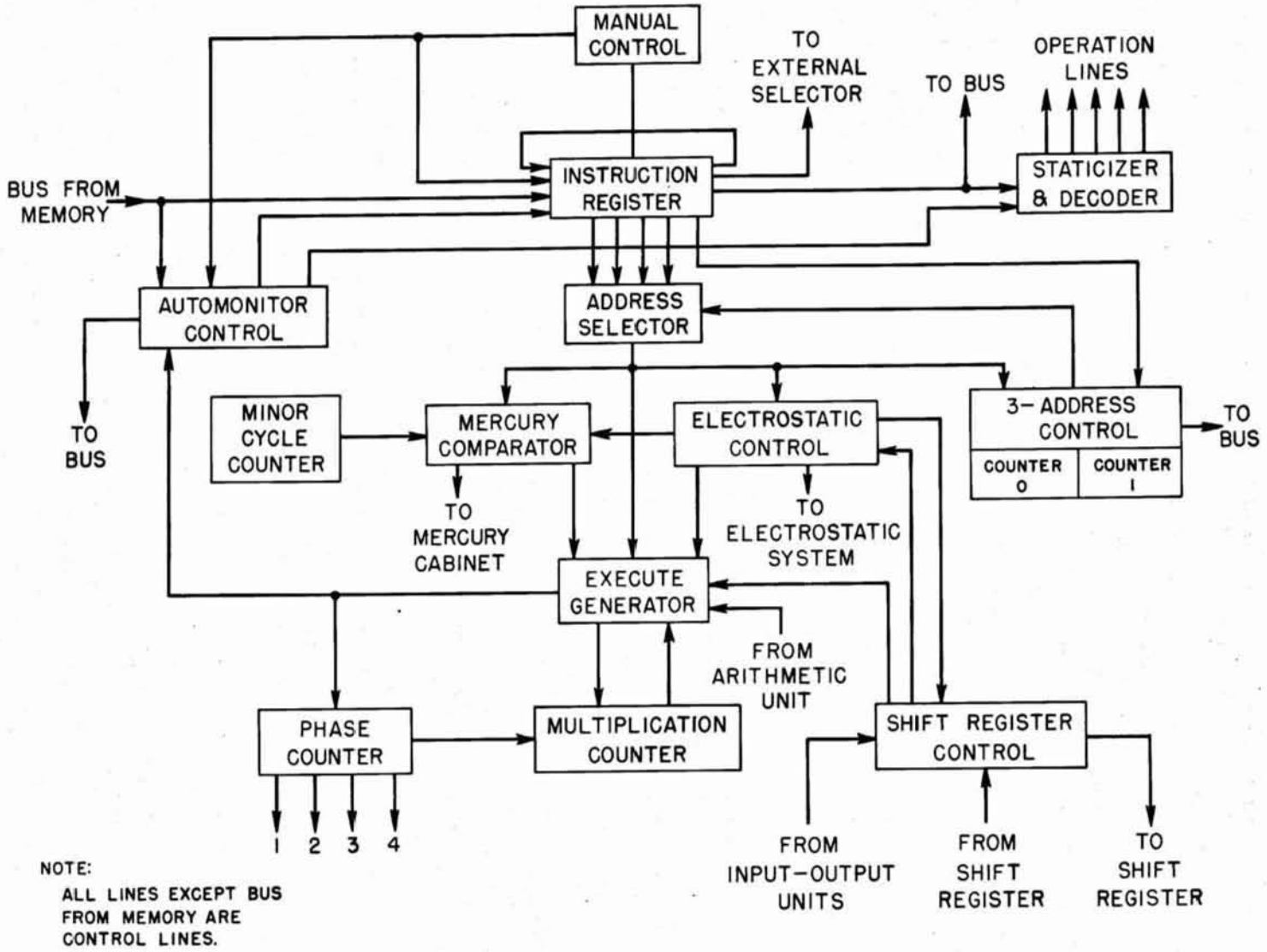

FIGURE 1.5. *Block diagram of Control Unit.*

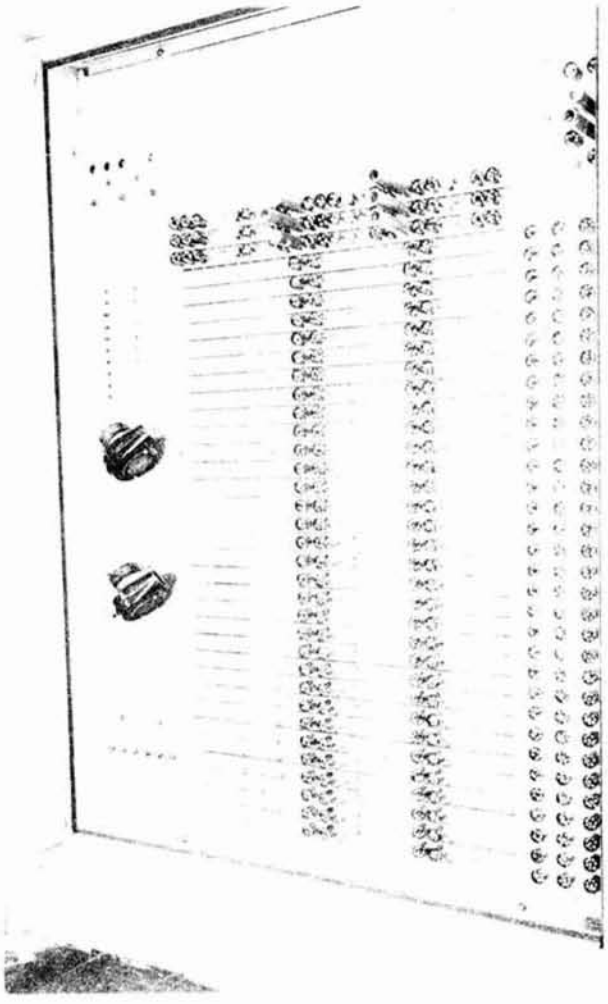

FIGURE 1.6. *Side view of Mercury Memory cabinet.*

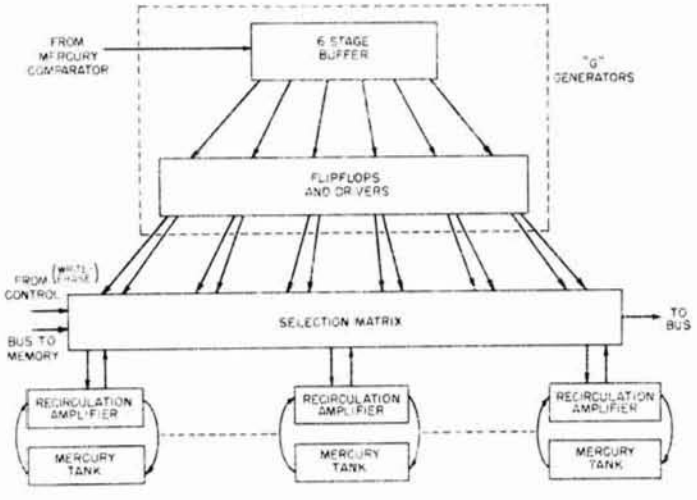

FIGURE 1.7. *Block diagram of the Mercury Memory.*

they can be simultaneously gated into six flip-flops with associated drivers. This portion of the circuitry is called access gating or, more popularly, "G" Generators. The varied combination of six positive and six negative pulse lines from the "G" Generators selects one of the 64 mercury lines that connect with the matrix. When writing into the memory, which is done in phase 4, information appears on the Bus to Memory, from which it is routed to the selected memory line, the old information being simultaneously deleted. In phases 1, 2, and 3, information from the selected address is transmitted via the output mixer of the matrix to the Bus. Information is erased by interrupting the recirculation path only when new information is written in.

As previously mentioned, in addition to the acoustic memory, SEAC also includes a full-scale experimental electrostatic memory. This provides an additional 512 words of storage, effectively increasing the capacity of the machine to 1,024 words. As this memory is arranged to operate in the parallel mode, the access time is considerably decreased, which thereby increases the speed of the machine over that which is possible with the mercury memory. The type of electrostatic storage is that originated by Williams and Kilburn, in which the phosphor surface of a conventional cathode-ray tube is charged to store digital information.

This memory occupies approximately six standard relay racks. Four racks hold the cathode-ray tubes (CRT) plus their associated regeneration amplifiers and gating circuitry. The remaining two racks contain the deflection generators, the counter, and other control circuitry. There are actually 48 CRT positions, but only 45 are employed at any one time. The other three positions are available as spares. Two types of cathode-ray tubes are used for storage, the 5UP1 and the 3KP1. The well-known dot-slide technique is used, in which a dot signifies a binary zero and a dash a binary one.

Figure 1.8 is a block diagram of the electrostatic memory for SEAC, showing the flow of information and the method of control. Numbers or instructions are transferred to the memory along parallel lines from the Shift Register, and this information is stored for as long as it is needed by a continuous process of regeneration, which takes place with the aid of the regeneration amplifiers. At any given time the location of the electron beam in the CRT is determined by the digital information in the Staticizer, which can be loaded from either the Address Register or the Regeneration Counter. The Staticizer sends out pulses of about 7-μsec duration. These pulses are sent to the Deflection Generators where they are decoded and converted to CRT deflection signals having very accurately derived voltage levels. All 48 CRT's are deflected in parallel, and the actions of turning the beam on and strobing the output signal of the amplifier are also performed simultaneously for all CRT positions.

The Operations Generator provides the proper "turn-on" signals to the CRT grids for both dot and dash conditions. It also provides a strobe pulse to the amplifier and a "twitch" signal to the Deflection Generators. The Synchronizer dispatches signals to the other units to insure that the correct sequence of pulses takes place and, furthermore, that these actions are synchronous with the rest of the machine.

When the electrostatic memory is being used, a read or write action can take place as frequently as every 48 microseconds. Of this time, only 12 μsec is actually required for the action, so the remaining time is always used to accomplish three regenerations.

The Shift Register and its Control comprise two full racks of equipment, which are shown in figure 1.9. Its size and complexity are due to its many functions. First, it acts as an intermediary, or buffer, storage between the input-output equipment and the serial acoustic memory. In connection with input-output operations, it also has the functions of digit counting, word counting, and word inversion. Further, the Shift Register acts as a register for the electrostatic memory, which operates in the parallel mode, and serves to provide the transfer to and from the serial representation in the rest of SEAC. In connection with the electrostatic memory, it also helps perform the logical transfer operation.

Figure 1.10 is a simplified diagram of the Shift Register showing how it connects to both memories. It will be noted that the register consists of 48 flip-flops arranged in a closed loop. Shifting may be done only to the right, as indicated by the arrows. During an input operation, the highest order of the number comes in first and is sent to stage 46. This digit then undergoes a

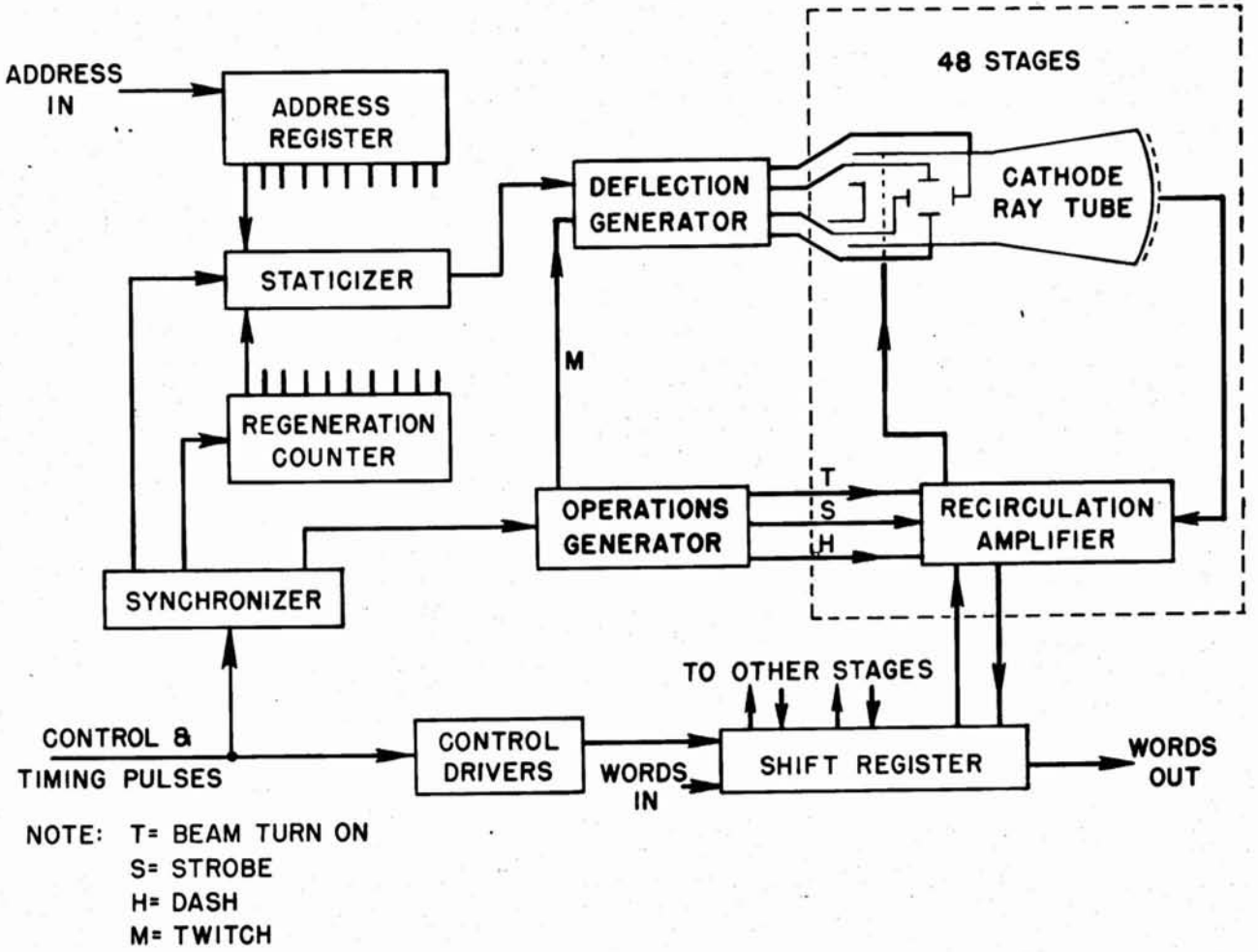

FIGURE 1.8. *Block diagram of the Electrostatic Memory.*

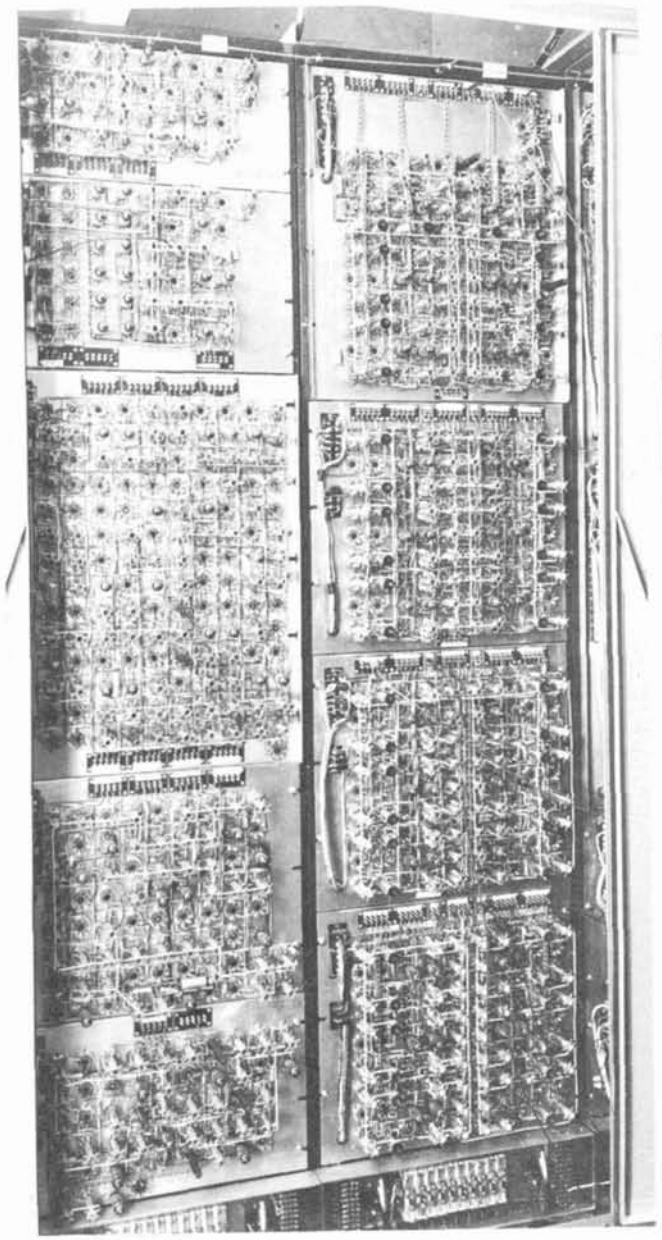

FIGURE 1.9. *Shift Register and Shift Register Control.*

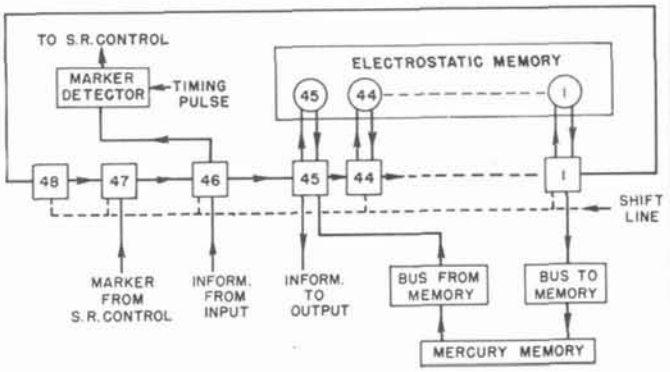

FIGURE 1.10. *Block diagram of Shift Register.*

series of right shifts, until it ends up in stage 47. Then the second highest order digit is inserted in stage 46, and again a series of right shifts takes place. This process continues until the entire number has entered the Shift Register. When the number is in position, a marker pulse signals the end of operation. At this time the number is shifted serially from stage 1 of the Shift Register into the memory at a one-megacycle rate.

During an output operation, the reverse process takes place. The number is shifted rapidly into the register through stage 45. Then, one digit at a time is sent to the appropriate tape, wire, or teletype unit via stage 45. The end of operation is again signalled by the marker pulse.

The Input-Output equipment used in SEAC is fully covered in a separate article. However, some salient facts pertaining to each type of equipment may be of general interest. The Teletype equipment operates at six characters per second, where each character represents four binary digits. This gives an equivalent speed of two seconds per word. Because of this low speed, Teletype is used primarily for manual operations, for which it is a very convenient means for printing out or inserting information in any memory location. The wire units, which employ cartridge loading, are used mainly for initial input and final output from the computer. The time required to fill the mercury memory from the wire input is about 12 sec, including the time for manual manipulations. The tape units developed at NBS for external storage use no reels and are single channel only. These units will hold up to 24,000 words on a 1,200-ft tape. Recently a multichannel tape unit was added to SEAC. Both types of tape units have extremely rapid acceleration, starting and stopping in less than 5 msec. This characteristic makes them especially valuable for external storage.

The Input-Output Selector (upper half of fig. 1.11) consists of the manual switches and the circuitry that are necessary to select one or more units for an input or an output operation. The system permits selection from among 10 different units. A unit may be selected automatically by inserting the proper information in the input or output instruction. The five binary digits that contain the necessary coding enter the Selection Register, as indicated in figure 1.12. The outputs of the register energize at least one selector relay (shown at the top of the diagram) by means of the Selection Gates and Automatic Selection Switches. These multicontact relays switch the necessary signals to control reading and writing on the unit. An input or an output instruction, of course, contains a code to designate a particular input-output unit; however, by means of manual switches on the Input-Output Selector one can establish any correspondence desired between the codes and the actual devices. This feature is especially useful when a new code is being checked or when one of the units happens to be inoperable.

The function of the Comparator is to determine when the input-output unit called for is different from the one previously chosen. Only in this situation is the computer halted momentarily while the necessary relays are energized. Automatic selection can be overridden by any of the manual selection switches. There are three of these switches, one for manual input operations, one for manual output operations, and one for direct selection during computation.

There are a number of auxiliary units physically separate from SEAC that allow the slow work of preparing input programs and data and that of printing the output results to be accomplished without losing valuable computing time. Teletype keypunches and reperforators are used to prepare the initial punched paper tape. An inscriber transfers the information from the punched tape onto magnetic wire for rapid computer input and automatically inserts the proper spacing between blocks of information. An outscriber takes the output data printed onto wire by the computer and produces a punched paper tape. This unit takes its information from a continuously moving wire, performs the necessary operations of counting and recognizing each binary digit, punches the paper tape, and checks for errors in the transcription to the wire as well as errors in its own operation. Additional equipment produces printed copy and/or punched cards from the tape punched by the outscriber.

Besides the fundamental requirements of starting and stopping the machine, the SEAC control console has many facilities that enable the operator to follow the course of the problem, print out any desired information, and make any changes that might be required. Only a few steps are required to put a new problem into the computer. These are clearing the control and memory, selecting the desired input unit, and pressing the start button. To perform a manual print out, the machine must first be halted by throwing the Run-Halt switch. The Computer then halts after performing the present instruction. The Print-Out switch is then positioned to allow the operator to print out either

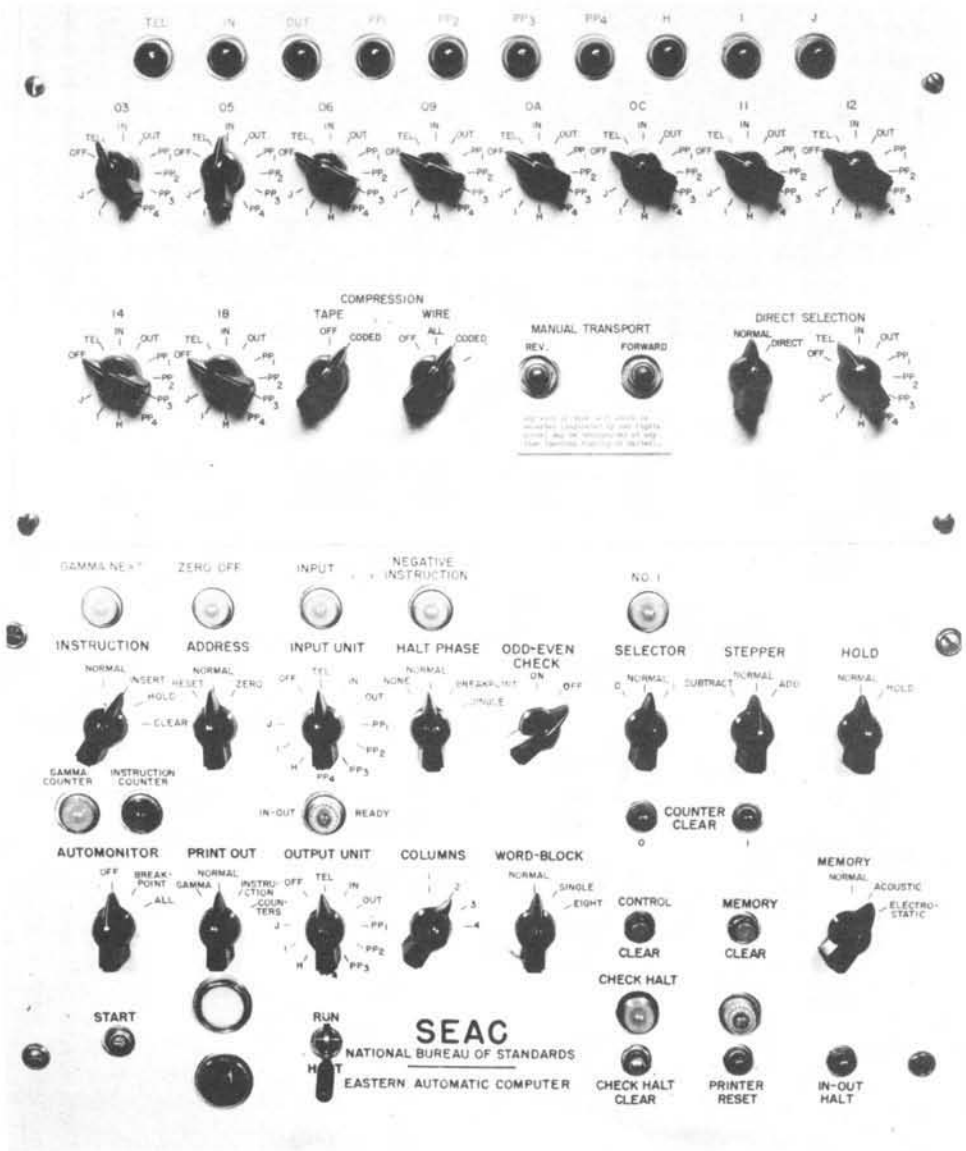

FIGURE 1.11. *Input-Output Selector panel and Manual Control Panel (bottom).*

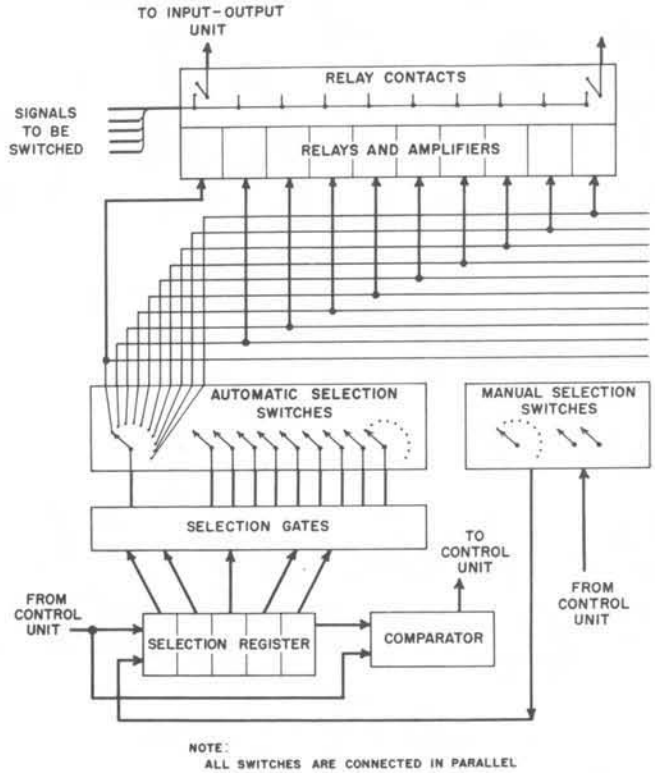

FIGURE 1.12. *Block diagram of Input-Output Selector.*

the instruction just performed, the result of the instruction, or the counter contents. The manual output selector switch allows the operator to select any unit, but the one usually chosen is Teletype.

To insert a word into any specified memory location, first the machine must be halted and the Instruction switch thrown to INSERT. When the Start button is pushed, an input instruction in which γ is the specified location is read into the first cell of the memory from the unit selected by the Input Selector Switch. Again the unit selected is usually Teletype. The Instruction switch is now set back to normal, the Start button pushed once more, and the operation completed. The memory Selector switch permits computation to be carried out in either the Electrostatic or Mercury Memory without a change in coding. In the Normal position of the switch, both memories are in use. The preceding discussion is by no means an exhaustive treatment of the switches and manual control operations available, but mentions briefly those most frequently used.

4. CIRCUITRY AND SYMBOLS

The circuitry of SEAC follows a rather uniform pattern throughout most of the central computer, with the exception, of course, of recirculation amplifiers, magnetic tape amplifiers, and the like. This pattern consists of diodes and resistors for gating, a beam power tube for amplification, and a transformer for coupling to subsequent stages. By intensive engineering of a single type of circuit, a high degree of reliability was achieved and subsequent design, testing, and maintenance were simplified.

Figure 1.13 shows a typical gating stage, of which there are numerous variations. Certain facts about the gating should be pointed out. The diode structure is three gates deep, or-and-or. Up to five inputs are allowed to each gate before the resistor values must be changed; however, this condition occurs in very few locations. The resistors are computed to allow a minimum rise of 100 v/μsec during any part of the pulse excursion. The diodes drawn in a horizontal direction carry pulse information; those drawn in a vertical direction are the clampers. It will be noticed that the gate output, which connects to the grid of the amplifier, is connected to a −5-v clamping diode. As the middle of the gate employs a −8-v clamping diode, a 3-v disconnect is obtained across the final or-gate. This is important in preventing noise from producing spurious signals. An additional disconnect of 2 v is achieved by connecting the positive output of the transformer to −10 v. Negative inputs to and-gates that are used for inhibition omit the initial or-gate, and the position of the −8-v clamping diodes is shifted to prevent them from drawing excessive current.

The single vacuum tube in the stage, tube type 6AN5, has no gating function. Its purpose is power amplification only. The 6AN5 is a miniature beam power tube with some excellent characteristics for this kind of computer service. Its pertinent characteristics are enumerated as follows:

Input capacitance	9.0	$\mu\mu$f.
Output capacitance	4.8	$\mu\mu$f.
Transconductance	8000	μmhos.
Filament rating	0.45 amp at 6.3 v.	

The cathode material is passive nickel, which apparently prevents the formation of interface. In the unpulsed condition the tube stands by with a current of at least 1 ma. The clamping diode to +2 v and a small resistor in the cathode circuit help keep the dissipations of the control and screen grids within ratings.

The transformer used for coupling has several advantages. It provides impedance matching between tube and load, it enables a single stage to transmit either positive or negative pulses, and it avoids the difficulties involved in dc coupling. A step-down ratio of either 5 to 1 or 7 to 1 is used in most SEAC circuits. In any case, the equivalent load presented to the tube is such as to cause the tube to bottom, i.e., to operate below the knee of the $e_p - i_p$ curve. This kind of operation results in almost uniform voltage output even though tubes with 2 to 1 variation in current capabilities are plugged into the same circuit. The cores of the pulse transformers in SEAC are grain-oriented silicon iron in 0.001-inch thick laminations.

As SEAC is a synchronous machine, it requires precise timing pulses to all its circuits to keep the various parts of the machine in step. This is accomplished by the use of a 1-Mc master clock

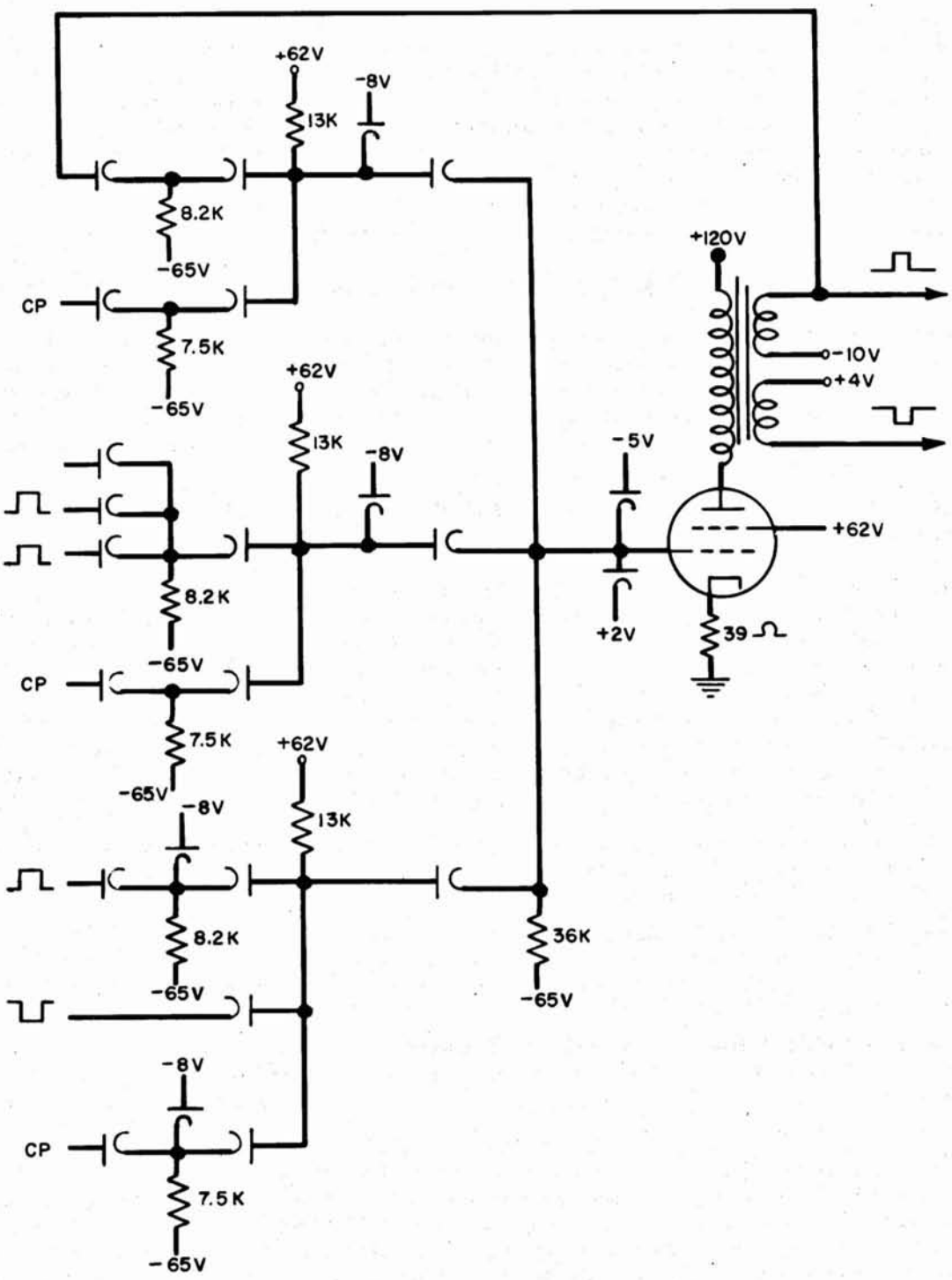

FIGURE 1.13. *Circuit of typical SEAC stage.*

which resembles a small radio-frequency transmitter. The clock signals are not distributed as rectangular pulses or half sine waves, as might be expected, but are full sine waves. There are definite advantages in using sine-wave distribution from the viewpoint of generation at high power levels, distribution without excessive pulse deterioration, and ease of phase shifting to produce the same precise timing in all parts of the computer. As the clock signal passes through the gating structure, only the trapezoidal center portion reaches the grid of the tube. These clock pulses are slightly under one-half microsecond at the top of the gating level. Although the computer could have been designed with a clock having only a single phase, the clock signals are actually distributed in three phases 120 degrees apart, which are named CP_1, CP_2, and CP_3. Because of the slight time delay in each SEAC stage and the overlap of successive clock phases, it is possible to send the output of a stage clocked with CP_1, for example, into the input of a stage clocked with CP_2 without the use of delay lines. Furthermore, three stages of gating may be done with only a 1-μsec delay. This is especially helpful in those parts of the machine where the time available to accomplish the necessary number of logical operations is limited. Figure 1.13 shows how the clock pulse is inserted into each and-gate.

A problem closely related to that of timing is that of pulse reshaping, so that the input signal on the amplifier grid is essentially a clock pulse. This may be accomplished by making sure that the incoming signals to any stage overlap both the leading and trailing edges of the particular clock phase used. As the incoming pulses will certainly be no broader than the clock pulses that produced them, delay lines may be used to achieve the necessary overlap. The method known as regeneration, which was devised shortly before the computer construction program began, accomplishes the same result without delay lines. All that is necessary in this method is that the pulses into a stage overlap the leading edge of the clock pulse. The positive output of the transformer is fed back as one of the inputs of the stage, and thus the pulse is held up until the trailing edge of the clock terminates it. The regeneration line is shown near the top of figure 1.13.

Electrical delay lines play several important roles in the computer. They are utilized in connecting stages where the clock phases are not consecutive; where a circulating register of any given length is required, e.g., the one-word Instruction Register; and where a pulse requires broadening, such as when a negative signal is used in an and-gate for inhibition.

The type of delay line used most generally in SEAC is of the continuous-wound design with an external ground shield. Lines of two different impedances are used: 1,350 ohms into a single gate and 800 ohms into two gates. The type of line used offers several advantages in this kind of computer service, viz., small space requirements, ability to be cut to exact value, satisfactory rise time for half-microsecond pulses, low temperature coefficient, and low attenuation. Delay line lengths in the computer vary from as little as 0.11 to 5.10 μsec.

One of the most frequently used circuits in any digital computer is the familiar Eccles-Jordan flip-flop. Its counterpart in the SEAC type of circuitry is called the dynamic flip-flop. This is not a flip-flop in the usual sense. Whereas the output of a conventional circuit has one of two d-c levels, the dynamic flip-flop output is considered to be in the "one" state when its output is a series of half-microsecond pulses and in the "zero" state when in the unpulsed condition.

The regular gating stage can be connected so as to become a dynamic flip-flop by returning the positive output of the transformer to the input through a delay line. By making the delay around the loop 1 μsec, there will be produced a continuous train of pulses until turned off. Only two and-gates plus a regeneration gate are required. The first gate can turn on the flip-flop with a single pulse, and the second gate serves as the recirculation path. The latter gate must also contain an inhibitor input to turn off the stage when desired.

Although the functions of a given chassis can be traced by using a detailed circuit diagram, this is often extremely arduous because of the maze of signal leads, resistors, tubes, and the like. A set of easy-to-follow symbols was developed during the preliminary period of computer design. These are shown in figure 1.14. As a tube is always associated with a transformer, a single symbol is used to denote both. A small circle indicates a negative output. Gates are symbolized by a closed semicircle, with the arc indicating the output side, thus eliminating the necessity for an arrow. And-gates are distinguished from or-gates by allowing the input lines to come up to the semicircle in the first case and through the semicircle in the second case. Negative pulse inputs

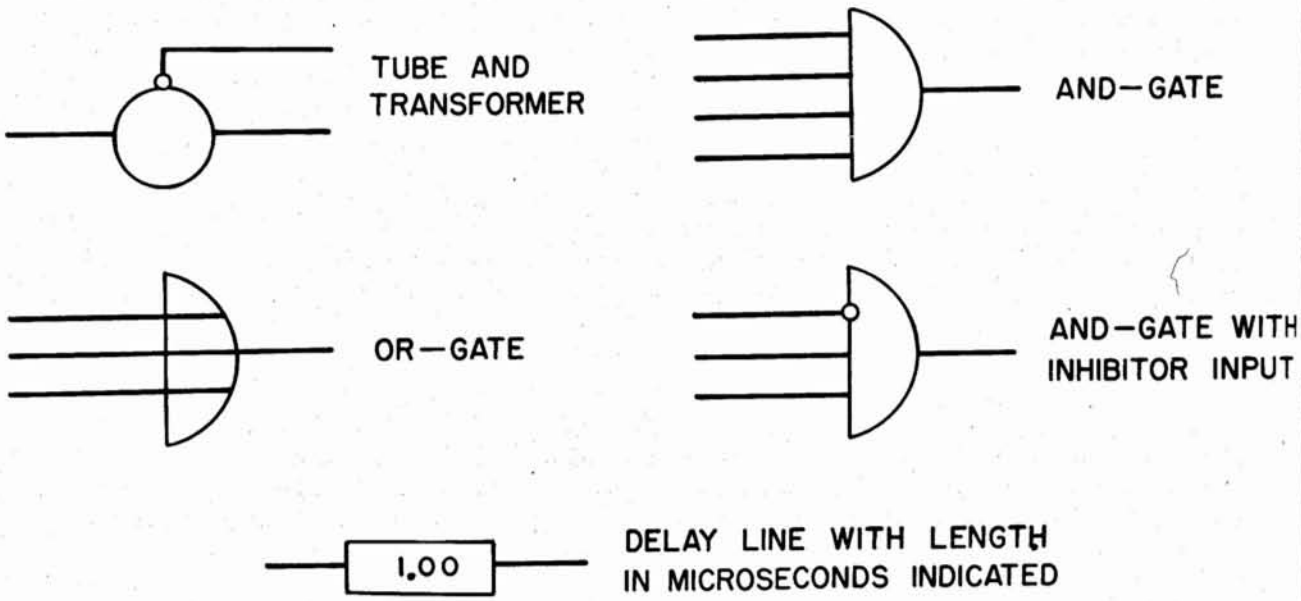

FIGURE 1.14. *Logical symbols used in SEAC.*

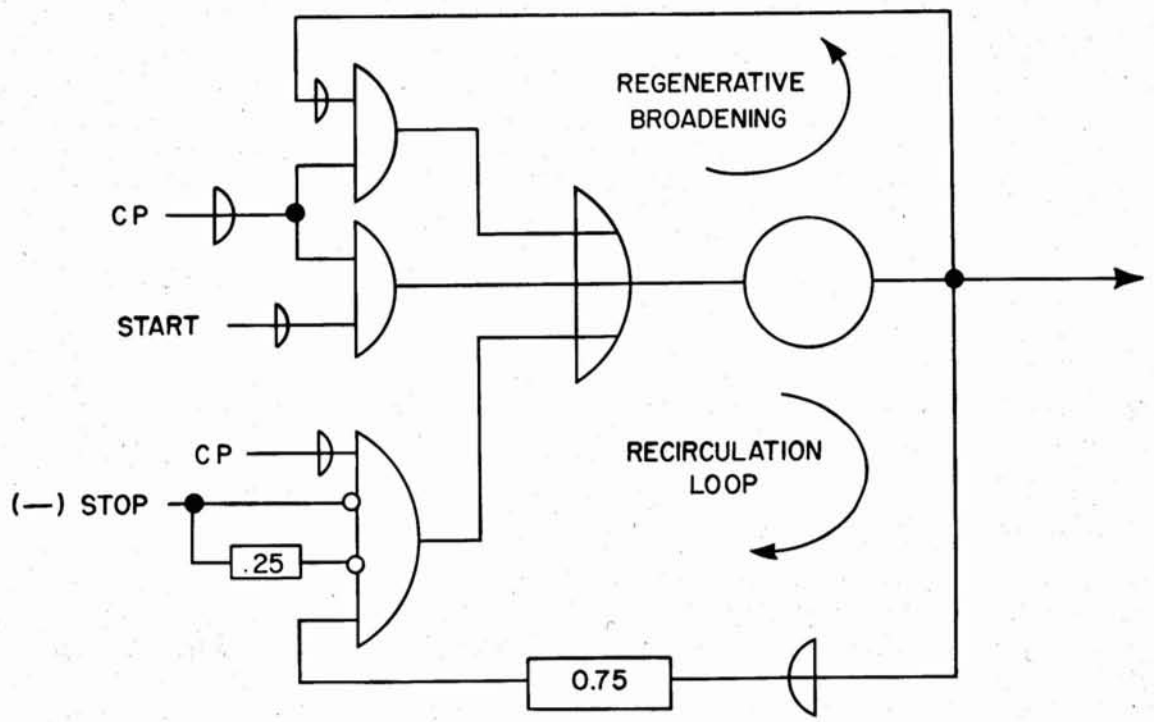

FIGURE 1.15. *Logical diagram of dynamic flip-flop.*

are again indicated by a small circle. Delay lines are symbolized by rectangles with the actual delay period indicated in the box. Figure 1.15 shows how these symbols are used in the logical diagram of the dynamic flip-flop just described.

Several advantages, some very obvious, have resulted from the use of a uniform circuit design. The fact that it allowed concentrated effort on a single type of stage has already been mentioned. Another advantage is that only one tube type is used, and tube selection is based on a single wide specification. The acceptable limits on plate current are 25 to 50 ma, with zero grid bias and +62 v on the screen and plate. These limits apply when checked with 5.7 v on the filament, as well as with 6.3 v. A tube is also rejected if there is an abnormal plate current variation when checked at the two filament voltage levels.

All diodes in SEAC are subject to the same specification, which, for initial installation, permits only 250-μa back current at 40 v and 2 v forward drop at 20 ma. Before a diode is removed the back current may increase to 500 μa.

It is possible to use unshielded wiring for distances up to 40 or 50 ft without encountering trouble from noise, because of the low effective impedance of the circuits. When the stage is pulsed, the tube-transformer combination presents a very low impedance. During the nonpulsed condition, it is the forward resistance of the -8-v clamping diode that furnishes the low impedance.

5. PHYSICAL CONSTRUCTION

Some of the over-all aspects of the physical construction of SEAC may be of general interest. The frame of the computer consists of two rows of nine standard relay racks (18 in all) with a walkway between. This arrangement does not include the mercury memory and the input-output equipment. When the computer was first put into operation, many of the racks were unfilled. This fitted in with the experimental nature of the machine and allowed for the expansion that was contemplated. At the present time the racks are completely filled by the additions that have since been made. On the interior, all plug-in components are easily accessible as are the interconnections between chassis. On the exterior, all chassis wiring, resistors, and tubes are also readily available. Thus any point on any chassis can be easily inspected either visually or electrically by means of oscilloscope or voltmeter. The accessibility is such that much of the early modification of circuits was done with the chassis in place.

Each relay rack has, on the average, four chassis of varying size. Filament and d-c power are made available at the bottom of each rack, where each line is fused individually. Power is transmitted from one chassis to another merely by plugging each chassis into the one below it.

The three-phase clock system is distributed in very much the same manner as the d-c power. Phasing controls and shaping circuits are provided on each rack for the individual clock phases. The shaping circuits are parallel L-C combinations located at both top and bottom of the rack to help maintain proper sine-wave form.

All signal outputs which must be sent from one chassis to another, are first terminated on a connector strip made especially for this purpose. This terminal strip is a rectangular piece of thin Bakelite on which are mounted pins similar to those used on an octal base, except that they are made available on both sides. For interchassis wiring, flexible insulated wire is used. Small female connectors that fit the pins on the terminal strip are mounted on either end.

Although the mechanical arrangement of components is not the same for all SEAC chassis and reflects the change in ideas that occurred during construction, the majority follow certain practices. Figure 1.16 shows both sides of a typical chassis. It will be noticed that tubes, resistors, and wiring are all located on one side, and the other components are on the other side. Everything except resistors and wiring is plug-in and is easily replaced.

The chassis are essentially two dimensional, although the use of turrets and plug-in components gives a certain amount of depth to the construction. This is achieved without any appreciable loss of accessibility, which is one of the main advantages of the two dimensional layout. Placing tubes and resistors on one side of the chassis and all other components on the other side separates the

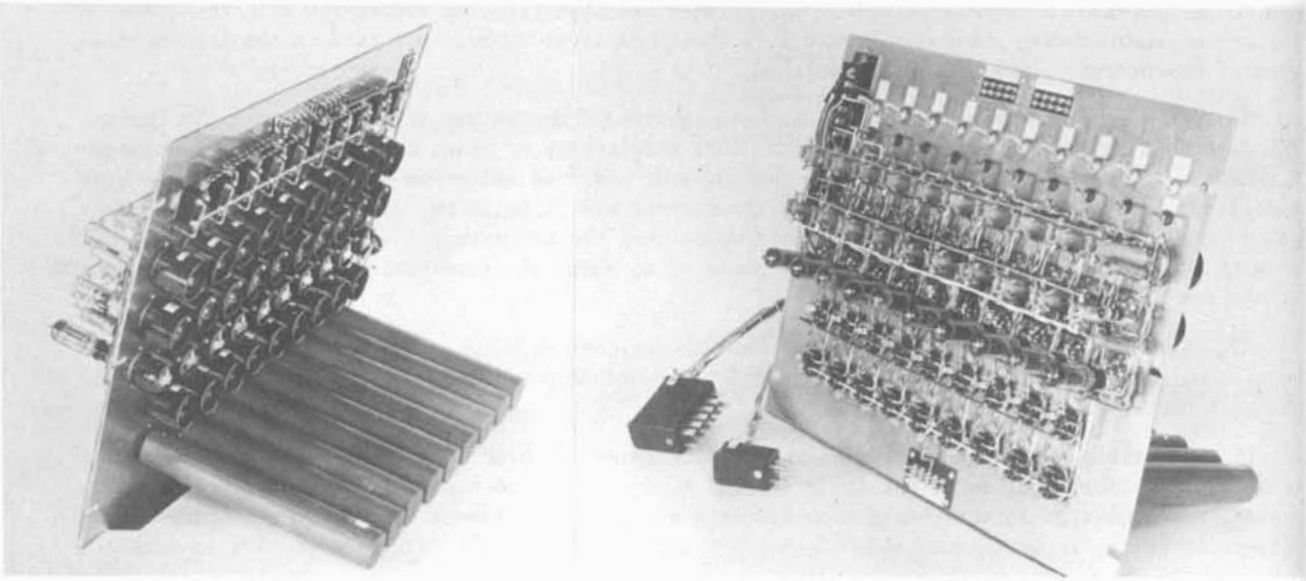

FIGURE 1.16. *Both sides of typical chassis.*

FIGURE 1.17. *Typical plug-in units.*

principal heat-generating elements from the heat-sensitive components, the most sensitive of which are the germanium diodes.

The plug-in components consist mainly of pulse transformers, electrical delay lines, and germanium diodes. Their construction is similar in that all use octal tube bases with solder-dipped connections. In figure 1.16 the first, second, and fourth rows are the diode clusters mounted in octal tube bases. The components in the third row are pulse transformers mounted in similar tube bases. The bottom row contains plug-in delay lines. These are made from a long length of delay line cut into sections of approximately the right length, which are then tailored to the desired value. When the electrical length of the delay line is not more than about 2 μsec, the line can be mounted in an octal tube base and covered with a protective Bakelite tube. Longer lengths of line are coiled in aluminum containers for mounting on the chassis. A more detailed view of typical plug-in units is shown in figure 1.17. The diode clusters, which comprise the majority of the plug-in units, consist of from 4 to 7 germanium diodes connected in a variety of ways. By restricting the number of diodes in a cluster to seven, each diode can be checked individually in the unit. As there are over 20 different types, there is sufficient choice to permit the straightforward layout of gating circuitry. When a cluster is rejected from the machine because of diode deterioration, the cluster is salvaged and only the bad diode (or diodes) is replaced.

Depending on their use, transformers are made with several different primary inductances and primary-to-secondary turns ratios. Originally, transformers were potted with a high-temperature wax compound, but later they were bracket-mounted to permit air cooling.

6. OPERATING PERFORMANCE

During most of its 3 years of operation thus far, SEAC has been in use 24 hours a day, 7 days a week. Regularly scheduled computation comprises the bulk of the 168-hour week, with smaller amounts given to routine maintenance and experimental engineering. During routine maintenance periods a continuing check of tubes and diodes is made such that all tubes are checked every 3 months and all diodes every 6 months. In addition, a system of marginal checking is used in which several of the more sensitive gating voltages are shifted up and down. Simultaneously, standard test routines are run and the point at which failure occurs is noted. Any poor tolerances that show up are investigated further. Several other items that are checked during the weekly maintenance period are (1) phasing of 1-Mc clock on each rack, (2) mechanical adjustment of Teletype equipment, (3) gain of Mercury Memory recirculation amplifiers, (4) condition of magnetic tapes.

A fair-sized library of routines has been accumulated for checking the Mercury Memory and various specific machine operations. However, except when unusual difficulties arise, use of two standard test routines is sufficient. One of these checks the memory for its ability to store several different pulse patterns; the other checks the ability of the Arithmetic Unit to perform the various operations. When an error occurs in either routine, the operator can usually diagnose the trouble by analyzing the information printed out.

In a machine as complex as any of the modern digital computers, the operator should be given, in procedure or machine facilities, any aid possible in checking codes and running problems. One of the procedures that has been used to great advantage with SEAC is summing of the memory. For example, after every read-in from magnetic wire, the machine is used to sum the information read-in, after which the sum is compared with the known correct ones. This enables the operator to know immediately whether or not the information has been correctly transferred into the memory.

The use of the sign in the instruction code to halt the computer has already been described. By manipulating one of the switches on the control console, the halt action can be modified in such a way as to help the operator check new codes. On one switch position the machine halts on all negative instructions, on the second position the machine halts only on negative print instructions, and on the third position the machine ignores all coded halts. If the operator uses negative instructions at strategic points (breakpoints), he can more quickly check the accuracy of his coding. Once the code is proved, he can then eliminate these breakpoints merely by throwing a switch without any necessity for changing his code.

Another valuable operator aid is the automonitor feature. The action of printing out the instruction, the result of the operation, and the counter contents is particularly useful when checking out a new code. The operator can set the automonitor switch so that all instructions are monitored or so that only negative instructions are monitored. If a code does not work the first time it is tried, the operator can automonitor the breakpoint instructions. By examining the information printed out, he can determine between what two points in the code the trouble occurred. He can then monitor all instructions between the two points and thus determine the exact point at which the program is in error.

The speed of various arithmetic operations in SEAC is given in table 2. This is arranged by acoustic and electrostatic memories.

TABLE 2

Operation	Time for complete operation, including access time (in milliseconds)			
	Acoustic memory			Electrostatic memory
	max	min	avg	
Addition	1.54	0.19	0.86	0.24
Subtraction	1.54	.19	.86	.24
Comparison	1.20	.19	.70	.19
a. Algebraic.				
b. Absolute.				
Logical transfer	1.54	.19	.86	.24
Logical multiplication	1.54	.19	.86	.24
Multiplication	3.65	2.30	2.98	2.35
a. Major part, unrounded.				
b. Major part, rounded.				
c. Minor part.				
Division	3.65	2.30	2.98	2.35
Base	1.20	.19	.70	.19
File	.86	.19	.52	.24
Clear	1.54	.19	.86	.24

An article on SEAC would be incomplete without some mention of the computation performed since the machine went into operation. During the past 3 years, hundreds of problems covering a wide range of applications have been run on SEAC. A list of broad categories of problems with a few examples in each category follows:

1. Mathematics and statistics:
   Table of Jacobi elliptic functions for real arguments.
   Solution of partial differential equations by Monte Carlo method.
   Generation of optimum sampling plans for the Bureau of the Census.

2. Physics problems:
   Crystal structure.
   Relative abundance of the elements.
   Wave functions for helium atom and for lithium atom.

3. Engineering problems:
   Optical system design.
   Synchrotron design.
   Starting transient in a class C oscillator.
   Transient stresses in aircraft structures.
   Plastic deformation of eccentric columns.

4. Business management and economic problems:
   Problems related to Air Force program planning.
   Problems related to social security accounting procedures.

5. Problems of a security classified nature for the Atomic Energy Commission and the Armed Forces.