THE
CONTROL DATA
6600
BASIC DESIGN CRITERIA

- INCREASE MEMORY SPEEDS & EFFICIENCY
- IMPROVE DATA THROUGH-PUT
- MINIMIZE INSTRUCTION FETCH DELAY
- ACHIEVE CONCURRENT INSTRUCTION EXECUTION
- USE STATE-OF-THE-ART TECHNOLOGY
CENTRAL MEMORY

CONTROL DATA 6600

131k or 65k
60 bit words
1μs cycle time
1 word/100 nanoseconds
transfer rate

Organized as:

- 32 banks each 4096 words
- Successive banks accessed every 100 nanoseconds
- Serial addressing guarantees successive bank references

<table>
<thead>
<tr>
<th>12 bits</th>
<th>5 bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>word address</td>
<td>bank</td>
</tr>
</tbody>
</table>

XXX00
XXX01
XXX02
XXX03
XXX04
XXX05
XXX06
XXX07
XXX10

Nanoseconds

0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0
CENTRAL PROCESSOR

CONTROL DATA 6600

24 REGISTERS
- 8-X REGS
- 8-A REGS
- 8-B REGS

IO FUNCTIONAL UNITS

INSTRUCTION STACK
8 - 60 BIT WORDS

CENTRAL MEMORY
65K OR 131K

24 REGISTERS - 3 ADDRESS CENTRAL PROCESSOR
INSTRUCTION FORMATS

- **15 BIT INSTRUCTIONS**
  - OP CODE
  - RESULT REGISTER
  - 1ST OPERAND REGISTER
  - 2ND OPERAND REGISTER

  ![Diagram of 15 bit instructions]

- **30 BIT INSTRUCTIONS**
  - OP CODE
  - RESULT REGISTER
  - 1ST OPERAND REGISTER
  - 2ND OPERAND REGISTER

  ![Diagram of 30 bit instructions]

DATA FORMATS

- **FLOATING POINT FORMAT**
  - SIGN EXP COEFFICIENT
  - S 11 48

  ![Diagram of floating point format]

- **FIXED POINT FORMAT**
  - SIGN INTEGER
  - S 59

  ![Diagram of fixed point format]
PERIPHERAL PROCESSOR

4096 WORDS
12 BITS
1\mu s CYCLE TIME

<table>
<thead>
<tr>
<th>A</th>
<th>18 BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>P</td>
<td>12 BITS</td>
</tr>
<tr>
<td>K</td>
<td>9 BITS</td>
</tr>
<tr>
<td>Q</td>
<td>12 BITS</td>
</tr>
</tbody>
</table>

64 INSTRUCTIONS
1\mu s MAJOR CYCLE

AVERAGE INSTRUCTION TIME = 2 MAJOR CYCLES

CONTROL DATA 6600

CENTRAL MEMORY
65K OR 131K
60 BITS

I/O CHANNELS

ONE OF TEN
INSTRUCTION FORMATS

- **12 BIT INSTRUCTIONS**
  
<table>
<thead>
<tr>
<th>OPERATION CODE</th>
<th>OPERAND OR OPERAND ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>6</td>
</tr>
</tbody>
</table>

- **24 BIT INSTRUCTIONS**
  
<table>
<thead>
<tr>
<th>OPERATION CODE</th>
<th>OPERAND OR OPERAND ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>p</td>
<td>p+1</td>
</tr>
</tbody>
</table>

DATA FORMAT

- **12 BIT DATA WORD**
  
  | 11 | 0 |
PERIPHERAL PROCESSOR CYCLE

CONTROL DATA 6600

M₀  M₁  M₂  M₃  M₄  M₅  M₆  M₇  M₈  M₉

CENTRAL MEMORY

READ PYRAMID

60 BITS

WRITE PYRAMID

12 BITS

I/O CONTROL
**EXCHANGE JUMP PACKAGE**

**CONTROL DATA 6600**

<table>
<thead>
<tr>
<th>LOC.</th>
<th>6</th>
<th>18</th>
<th>18</th>
<th>18</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>P</td>
<td>A0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n+1</td>
<td>RA</td>
<td>A1</td>
<td>B1</td>
<td></td>
</tr>
<tr>
<td>n+2</td>
<td>FL</td>
<td>A2</td>
<td>B2</td>
<td></td>
</tr>
<tr>
<td>n+3</td>
<td>EM</td>
<td>A3</td>
<td>B3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A4</td>
<td>B4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A5</td>
<td>B5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A6</td>
<td>B6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A7</td>
<td>B7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- X0  
- X1  
- X2  
- X3  
- X4  
- X5  
- X6  
- X7  

P = PROGRAM ADDRESS  
RA = REFERENCE ADDRESS  
FL = FIELD LENGTH  
EM = EXIT MODE
PERIPHERAL EQUIPMENT

6602 CONSOLE

- 2-10" DISPLAYS
- 16-32-64 CHARACTERS/LINE
- CHARACTER OR DOT MODE
- A/N KEYBOARD ENTRY

405-B CARD READER

- 1200 STD CARDS/MIN.
- BUFFER
- CODE TRANSLATION

415-B CARD PUNCH

- 250 CPM
- ROW PUNCHING

607-B MAGNETIC TAPES

- 150"/SEC.
- 200/556/800 BPI
- 120 KC TRANSFER RATE
- BINARY OR BCD MODES
- HALF-INCH WIDTH

6603 DISC

- 80 M CHARACTERS CAPACITY
- 1100/1400 KC
- 12-BIT TRANSFER
- 33 MS AVG. ACCESS WITHIN TRACK
- 240 MS MAX. HEAD POSITIONING

501-B PRINTER

- 1000 LPM
- 136 CHARACTERS/LINE
- 64 CHARACTER SET
- BUFFERED

626-B MAGNETIC TAPES

- 150"/SEC.
- 800 BPI
- 240 KC TRANSFER RATE
- BINARY MODE
- ONE-INCH WIDTH
128 TRACKS PER SECTOR

4 ZONES (1,2,3 AND 4)

TRANSFER RATE
1100-1400 KC

128 SECTORS EACH
ZONES 3 AND 4

351 BITS PER TRACK

4 HEADS
PER SURFACE

RECORDING—
12 BIT
PARALLEL

100 SECTORS EACH
ZONES 1 AND 2

HYDRAULIC
ACTUATOR

12 DISC - 24 SURFACES
80 M CHAR. CAPACITY
33 MS. AVG. ACCESS (TRACK)
240 MS. MAX (POSITIONING)
SYSTEMS COMMUNICATIONS

CONTROL DATA
6600

PROGRAMMING CONSOLES

OPTICAL DATA READERS

I/O STATIONS

ANALOG

6600 COMPUTING FACILITY

MICROWAVE COMMUNICATIONS TERMINAL

LONG LINE COMMUNICATIONS TERMINAL

DATA COLLECTION EQ.
SOFTWARE

CONTROL DATA
6600

6600 COMPUTER SYSTEM PROVIDES:

- UNPRECEDENTED COMPUTATIONAL POWER
- MULTI-PROCESSING CAPABILITIES

6600 SOFTWARE:

- INTEGRATES HARDWARE FEATURES
- RESULTS IN AN UNMATCHED LEVEL OF THROUGHPUT
SIPROS FEATURES:

- DISC - ORIENTED I/O SYSTEM
- PARAMETRIC DESIGN
- MULTI-LEVEL PRIORITY SYSTEM
- INTERNAL JOB SCHEDULING
- JOB ACCOUNTING
- PROGRAM PROTECTION SAFEGUARDS
- DYNAMIC MEMORY ALLOCATION
- PPU TASK ASSIGNMENT
- HARDWARE DIAGNOSTIC ROUTINES
- OPERATOR INTERVENTION ABILITY
- VISUAL DISPLAY OF SYSTEMS ACTIVITY
FORTRAN 66

FORTRAN IV EXTENDED
PRECISION 15/29 DIGITS
MAGNITUDE - $10^{\pm308}/2^{59-1}$
DISC READ-WRITE
COMPILE MODE OPTION
REGISTER REFERENCE OPTION

INTERMIX FORTRAN 8 ASCENT CODE
SEGMENTION FEATURE
FORTRAN CONSTANT NOTATION
FORTRAN TYPE DECLARATIONS
FORTRAN LIBRARY Routines

HARDWARE-ORIENTED SYMBOLIC ASSEMBLER
SYSTEM MACROS FOR I/O OPERATIONS
PROGRAMMER-DEFINED MACROS
EXTENSIVE PSEUDO-OPS
MULTI-STATEMENTS PER LINE

ASCENT
SOURCE LANGUAGE

ASPERS

- MACHINE-ORIENTED MNEMONICS
- PSEUDO-OPS
- SYSTEM INPUT-OUTPUT MACROS
- SEGMENTATION FEATURE
- CENTRAL MEMORY BLOCKS RESERVATION
- SYSTEM CHANNEL SCHEDULING MACROS
- ACCESS TO ASCENT SYMBOLS

CONTROL DATA

6600
SYSTEM COMPONENTS

CONTROL DATA 6600

POOL PROCESSORS

EXECUTIVE AND MONITOR PROGRAM

CENTRAL MEMORY

DISC EXECUTIVE PROGRAM

SYSTEM DISC
DISC ORGANIZATION

SYSTEM DISC FUNCTIONS
- PROGRAMMER SCRATCH AREA
- JOB STACK
- OUTPUT BUFFERS
- SYSTEM Routines

VARIABLE LENGTH LOGICAL RECORDS

<table>
<thead>
<tr>
<th>PROGRAMMER SCRATCH AREA</th>
<th>JOB STACK</th>
<th>OUTPUT BUFFERS</th>
<th>SYSTEM Routines</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>J1</td>
<td>01</td>
<td>S1</td>
</tr>
<tr>
<td>P2</td>
<td>J2</td>
<td>02</td>
<td>S2</td>
</tr>
<tr>
<td>P3</td>
<td>J3</td>
<td>03</td>
<td>S3</td>
</tr>
<tr>
<td>P4</td>
<td>J4</td>
<td>04</td>
<td>S4</td>
</tr>
<tr>
<td></td>
<td>J5</td>
<td>05</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>06</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>07</td>
<td></td>
</tr>
</tbody>
</table>

SYSTEM DISC

P1 S4
P7 S5
P6 S6
P3 S3
P5 S2
P4 S1
P2 S0
DECK ORGANIZATION

* END OF JOB CARD

DATA

PROGRAM

OPTIONAL

MEMORY MAP
DUMP ADDRESS
SNAP DUMP
CONSOLE REQUIREMENTS
ERROR HALT CONDITIONS

OPTIONAL

TAPES
PERIPHERAL PROCESSOR
PROGRAMS
DISC ESTIMATE
MEMORY ESTIMATE
EQUIPMENT CHANGES

REQUIRED

*JOB NAME
*ACCOUNT NUMBER
PRIORITY
TIME LIMIT

OPTIONAL

* INDICATES REQUIRED INFORMATION
CPU Programming Guidelines

Control Data 6600

- An instruction may be issued if:
  1. The previous instruction has been issued, and
  2. The functional unit required is free, and
  3. The result register required is free

- An instruction may begin execution if:
  1. It has been issued, and
  2. All other registers required are free

- Representative execution times

  Address incr. 3*  
  FLT. ADD 4  
  FLT. Multiply 10  
  Branch 8  
  FLT. Divide 29  
  Read from mem. 8  
  Write into mem. 10

* All times in minor cycles