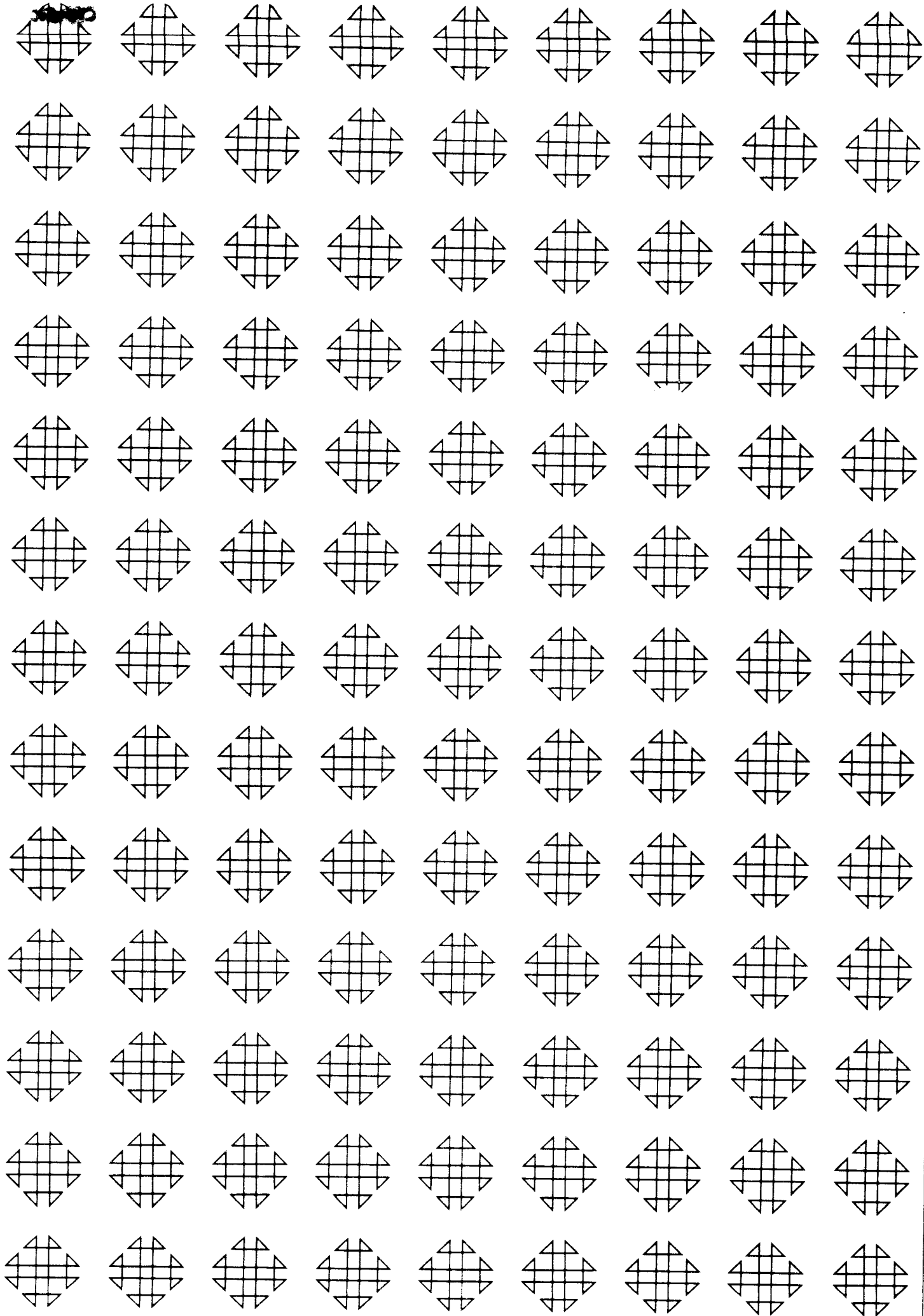


*f. sturmf*  
**1401 GENERAL PROGRAM LIBRARY**

SCION (Scientific 1401 Programming with Floating Point) 3.0. 002



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Title: SCION II ( Floating Point for 1401 Systems )  
Author: John Discola  
IBM - Los Angeles East  
6252 East Telegraph Road, Los Angeles 22, California

Date: August, 1961

Purpose: A. SCION II provides the programmer with the ability to generate - with one system deck - a complete source program deck containing customized floating point operations ready for SPS assembly. In particular, the SCION system will process a preliminary SPS program containing floating point macro-type instructions and create linkages to the floating point subroutines which are themselves generated initially by the system deck. These subroutines are customized in regard to the size mantissa to be used and the compilation - on a "call" type basis - of the subroutines required by the source program. Also compiled optionally is a tracing routine to aid in debugging whose operation at object time is controlled by the source program.

The mantissa sizes that may be compiled range from 4 digits to 16 digits by increments of 2 - viz. 2-4, 2-6, 2-8, 2-10, 2-12, 2-14, and 2-16 characteristic-mantissa type floating point format.

The arithmetic operations are FAD, FSB, FMP, and FDV. Mode conversion operations included optionally are floating-to-fixed ( FIX ) and fixed-to-floating ( FLT ) conversions. Their capabilities are 3 and 2 times the mantissa size, respectively.

B. SCION II avails to the programmer desirous of maximizing execution efficiency attendant "one-for-one" SPS coding and/or does not have the 1401 Fortran hardware configuration.

Equipment Specifications

IBM 1401 Model B, C, D, E, or F with the following special features:  
1. Multiply-Divide  
2. Advanced Programming

Source Language:

SPS II

C. Two digit characteristic ( excess-fifty mode ) gives the following range for floating point arithmetic operations:

$$.1000..0 \times 10^{-50} \text{ to } .9999..9 \times 10^{49}$$

Accuracy: Subroutines truncate significant digits of results after normalizing.

D. Storage Requirements:

All operations plus tracing  
no. positions =  $939 + 6 \times \Delta n$ ; where  $\Delta n = n - 4$ ; and  $n = \text{mantissa size}$

F. SCION subroutines are not restricted to memories larger than 4K since the Modify-Address (MA) instruction peculiar to the larger memory configurations is not used in any of the subject routines.

Index registers 1, 2, and 3 are used by the subroutines. This should not concern the programmer because they are restored to their entry conditions at exit time. One proviso is made however, namely - that word marks are not left in their tens and units positions at entry time.

SCION II SYSTEM FLOWCHART

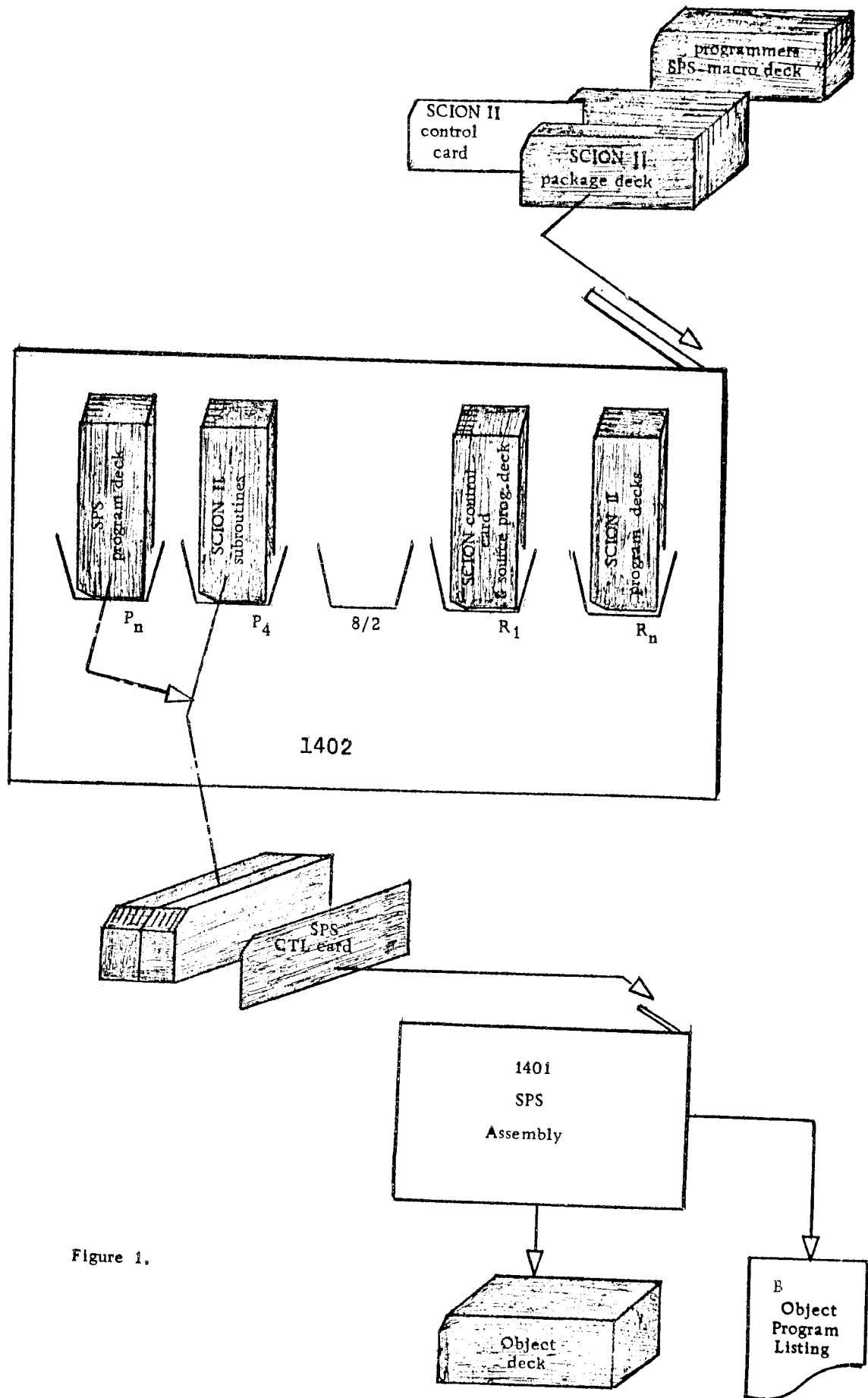


Figure 1.

## 1. The SCION System

The expressed purpose of this system is to avail to the programmer coding an application for the 1401 the ability to incorporate into his program "tailored" floating point operations with a minimum of difficulty. In particular, the programmer may make a determination of the optimal mantissa field size required by the algorithm of an application in order to maximize execution efficiency and available memory work-area space. It should be noted that this is not possible with fixed word length type computers.

SCION II provides this capability as its primary function in addition to allowing macro-type coding of floating point operations in the mother SPS language. Including assembly, the system (source to object program) may be considered a two pass proposition.

The first pass is the SCION pass which requires only the system deck, a control card, and the source program with macro instructions. This pass initially generates a deck of floating point subroutines in symbolic form based on the specifications indicated in the

### A. Subroutine Generation

The SCION control card specifies mantissa size ( nn ) in card columns 6,7. Actually the sizes possible range from 4 digits to 16 digits by increments of 2. Considering the 2 digit characteristic they are nominally: 2-4, 2-6, 2-8, 2-10, 2-12, 2-14, and 2-16.

Six floating point operations are available in SCION II - four are the arithmetic operations of addition, subtraction, multiplication, and division ( FAD, FSB, FMP, and FDV ). The remaining two are fixed-to-floating and floating-to-fixed mode conversion operations ( FLT and FIX ). Two or more of these individual operations may be compiled on a "call" type basis. However, the arbitrary selection of combinations of particular operations is not entirely possible because of the dependence of some routines to others. Figure 2, illustrates figuratively these dependencies and indicates the control card constant ( p ) to be punched card column 8 specifying the scope of operations to be compiled. For example, p=5 will compile all the operations.

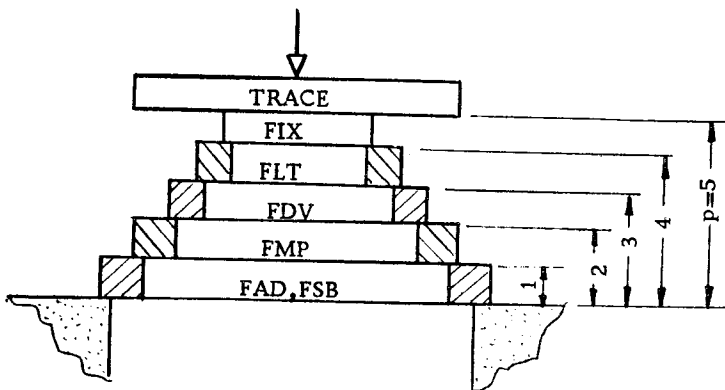


Figure 2.

control card. It then processes the source deck - reproducing it exactly except for the macro instructions, in which case it generates two legitimate SPS instructions that represent the linkage to the aforementioned subroutines. It simultaneously produces a 1403 listing of the resulting symbolic source program with annotations indicating errors in macro coding.

The SCION control card designates three things to the processor: the mantissa size, the number of routines required, and whether or not a special tracing routine is to be compiled with the routines.

The tracing feature may be of invaluable assistance in the debugging of the program without the use of a great deal of 1401 time because of a selective tracing option that is programmable in the source program.

The cards produced from the SCION pass can be used immediately for SPS assembly without the addition of any other supplementary decks. Figure 1 illustrates diagrammatically the two passes described above.

The tracing feature that may be compiled with the operations is called by TRACE in the SCION control card in card columns 9-13. This routine does not become functional at object time until an instruction in the source program "turns on" the trace. This instruction is symbolically in the source program:

```
### ##### #####
B  TRACON
### ##### #####
```

Upon encountering any floating point operations following this instruction the print area will be cleared and the following information is printed at the 1403 after execution of the operation:

1. floating point pseudo operation code
2. actual A-field address
3. actual B-field address
4. contents of A-field
5. contents of B-field
6. contents of answer field ( AC ) or contents of FIX field ( REG )
7. NSI ( next sequential instruction )  
eg. BXXX

All subsequent floating point operations will be traced until another instruction is executed which turns the trace off, and it is symbolically:

```
### ##### #####
B  TRCOFF
### ##### #####
```

The output of the sample program of Section III illustrates the use, results, and format of the trace operation.

## B. Macro Instructions and Linkage

The second function of the SCION system is to re-create the source program and to substitute two entry instructions for every macro-type floating point instruction that is encountered in the original source program. This entry and linkage to the subroutines is performed ostensibly by two SPS instructions - viz.

```
### ##### #####  
B SCION  
op AAA BBB  
### ##### #####
```

The second instruction ( 7 characters ) in reality is the entry data that designates the operation type and the two data addresses. It should be noted that this instruction is not executed. The linkage created within the routines returns at exit time to the first position following this "dummy" instruction. This should imply immediately that this position must contain a valid operation code with word mark to preclude a Process Error Stop.

The following is an epitomy of the functions of this portion of the first pass in addition to the creation of the aforementioned entry instructions:

1. reproduce all normal SPS information per card in their normal sequence.
2. reproduce the supplementary fields of the macro instruction into the first of the entry instructions.
3. Increase the line count by 1 and create an abbreviated form of the source macro instruction into comments field of the second entry instruction.
4. Check for invalid macro operation codes.
5. Simultaneously print an image of each SPS card produced.

Certain symbolic labels and addresses will common to both the subroutines and the source program in order to afford a working correspondence between the source program and the subroutines. All results of floating point operations are left in one of two fixed fields in SCION. These fields are addressed AC and REG and their explicit functions are outlined in Section II. Three labels also have correspondence with the source program - TRACON, TRCOFF, and SCION. The index registers #1, #2, and #3 are defined by DCW's - X1, X2, and X3, respectively.

## II. The Floating Point Operations

### A. Form of Data

The form of the floating point data word/field used and accommodated by the SCION subroutines is similar in nature to earlier schemes that have been used. The word/field consists of a two digit characteristic in the "excess-50 mode" and a mantissa which may be one of seven sizes as indicated previously. The range of the mantissa is  $-1.0 < M < 1.0$

eg: 324.56789 is represented in memory as:

5332456789 ( .32456789 x  $10^3$  )

One should note that the ordering is characteristic-mantissa which is logically more desirable. This ordering allows simplified and faster methods for the determination of relative magnitudes between datum.

### B. The Operations

Six floating point operations are provided in the SCION package. These operations differ in method somewhat from the normal 1401 arithmetic operations in which the result is left in the B-field thereby destroying the contents of one of the operand fields. The result of any SCION operation is left in a fixed field AC located within the memory space reserved by the subroutines ( except for the FIX operation ). The answer field AC is addressable in the source program and may used as the operand of any other instruction.

#### 1. Floating Addition and Subtraction

FAD/FSB AAA+/- BBB  $\rightarrow$  AC

The mantissa answer field is a result of truncation subsequent to normalization within this field. A positive mantissa is always left unzoned in AC.

#### 2. Floating Multiply

FMP AAA x BBB  $\rightarrow$  AC

A  $2(N_m)$  product field is developed and truncated as in 1., where  $N_m$  is the mantissa size.

#### 3. Floating Divide

FDV AAA / BBB  $\rightarrow$  AC

A  $(N_m+1)$  quotient is developed and truncated as in 1.

Note: In all of the arithmetic operations indexing is allowed. Indexing of the A-operand of the following FLT and FX operations is also allowed except when using index register #3.

The sign of the mantissa is always associated with the units position of the word/field and conforms to the sign or zoning standards of the 1401.

The following are the stipulations that are made concerning the condition of the floating point operands upon entry to the arithmetic operations:

1. Word marks must not exist in any position of the operand following the high order position of the field. A word mark in the high order position is optional.
2. The units position of the operand field should be zoned with a B-bit for negative datum.
3. The operand address of the floating point instruction should always be that of the units position of the field.

#### 4. Fixed-point to Floating-point Conversion

FLT AAA, L  $\rightarrow$  AC, where L is a literal placed left-justified in the symbolic B-field which specifies the number of A-field decimal places.

The maximum length of "unword-marked" A-field that may be floated is  $(2N_m)$ . Truncation and normalization are as in 1.

It should be noted that the decimal point in the A-field is an assumed position; that is, it does not physically exist as a memory position.

#### 5. Floating-point to Fixed-point Conversion

FIX AAA, L  $\rightarrow$  REG, where L is a literal placed left-justified in the symbolic B-field which specifies the number of REG-field decimal places.

The size of the REG-field which is left with the fixed data is  $(3N_m+1)$ .

All data that exceeds the capacity of the REG field will be placed right-justified in the REG field in the original floating point form with the character X separating the characteristic from the mantissa.

Note: Concerning blank or partially blank fields - no guarantee is given for proper operation should blanks exist in any operand field except for the FLT instruction. Blanks are legitimate in the A-operand field in this operation and the resultant AC field will not be left with blanks.



C. Example Results of Floating Point Operations

Assume the following data fields in memory:

5110000000<sub>A</sub> 5099999999<sub>B</sub> 5033333333<sub>C</sub>  
5066666670<sub>D</sub> 5555555555<sub>E</sub> 9876543210<sub>G</sub> 0000000000<sub>F</sub>

Macro Op Code	A-field Address	B-field Address	XXXXXXXXXX A C	XXXXXXXXXXXXXXXXXXXXXXXXXXXX R E G
FAD	A	B	5119999999	
FAD	A	C	5066666670	
FAD	AC	D	0000000000	
FSB	B	A	4410000000	
FSB	E	AC	5555555555	
FMP	B	C	5033333333	
FMP	E	G	9999999999 (1)	
FMP	F	AC	0000000000	
FDV	C	B	5033333333	
FDV	F-4	G	0000000000 (2)	
FDV	E	F	9999999999 (3)	
FLT	G	8	5855555598	
FLT	D-4	3	5350666600	
FIX	C	5		000000000000000000000000033333
FIX	E	20		555555550000000000000000000000
FIX	E	10		00000000055555555500000000
FIX	G	0		000000000000000076543210X98

- (1) Characteristic Overflow...see Section IV. A.
- (2) Characteristic Underflow...see Section IV. A.
- (3) Division by Zero.....see Section IV. B.

### III. Sample Problem

#### SPS Listing of Sample Problem Input

```

1010 * THE FOLLOWING IS A PROGRAM DESIGNED TO
1020 * ILLUSTRATE THE USE OF SCION AND TO
1030 * CORROBORATE THE OPERATION RESULTS SHOWN
1040 * ON PAGE 4 OF THE SCION WRITEUP.
1050 *
01 060      START  CC
01 070      MCW  OPCODE          0209
01 080      MCW  AFLD            0226
01 090      MCW  BFLD            0247
01 091      MCW  ACFLD           0272
01 100      MCW  NSI             0295
01 120      CC
*01 110      W
01 130      CS   0295
01 140      R   TRACON
01 150      FAD  A                R
01 160      FAD  A                C
01 170      FAD  AC               D
01 180      LABEL FSR R           A
01 190      FSR  E                AC
01 200      FMP  B                C
02 010      FMP  F                G
02 020      FMP  F                AC
02 030      FDV  C                B
02 040      FDV  F      - 4       G
*01 050      FDV  E                F
02 060      FLT  G                R
02 070      FLT  D      - 4       3
02 080      FIX  C                5
02 081      FIX  E                20
02 090      FIX  E                10
02 100      FIX  G                0
02 110      FXP  G
02 120      B   TRCOFF
02 130      H   START
02 150  10  A   DCW  *   5110000000
02 160  10  B   DC   *   5099999999
02 170  10  C   DC   *  -5033333333
02 180  10  D   DCW  *  -5066666670
02 190  10  E   DCW  *   5555555555
02 200  10  G   DC   *   9876543210
03 020  10  F   DC   *   0000000000
03 030  03  NSI DCW  *   NSI
03 050  07  AFLD DCW  *   A-FIELD
03 050  07  BFLD DCW  *   B-FIELD
03 051  12  ACFLD DCW *   AC-FIELD/REG
03 060  10  OPCODE DCW *   OP  A  R
3070 *NOTE SCION CONTROL CARD *SCION085TRACE*
3080 * LOCATED AFTER PACKAGE DECK =1
03 090      END  START

```



III. SPS Post-List of Total Program after Assembly, Page 1 of 4

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CLEAR STORAGE 1 ,00B015,022026,030034,041,045,053,0570731026  
 CLEAR STORAGE 2 L072116,11C106,10511781017199,027A074028B027B0010270B026/0991,001/00111710  
 ECCTSTRAP CARD ,00B015,022C29,056063/056027 ,0240671056

PC	LIN	CT	LABEL	OP	A OPERAND	B OPERAND	D	LOC	INSTRUCTION	COMMENTS
	01			CTL	33					
	02	3	X1	DCW	0333					AUG61
	03	3	X2	DCW	0089			0089		
	04	3	X3	DCW	0094			0094		
	05	3	X3	DCW	0099			0099		
	06	24	WPKZZZ	DCW	*			0333		
	07	10	REG	CC	*			0357		AUG61
	08	10	PFZZZZ	DCW	*			0367		
	09	10	CFZZZZ	DCW	*			0377		
	10	10	AC	DCW	*			0387		
	11	4	SCIGN	SBR	*	E 19		0388	H 410	AUG61
	12	4		MOW	X3		BOXZZZ	0392	M 099	873 AUG61
	13	4		MOW	X2			0399	M 094	AUG61
	14	4		MOW	X1			0403	M 089	AUG61
	15	4		MOW	0000		CPZZZZ	0407	M 000	577 AUG61
	16	7		SAR	X3			0414	C 099	AUG61
	17	7		SW	0005	3	0002	0418	M 065	062 AUG61
	18	7		MOW	C007	3	ALRZZZ-	0425	M 067	457 AUG61
	19	7		MOW	C004	3	ALRZZZ-	0432	M 064	464 AUG61
	20	4		MA	0009	3		0439	M 069	AUG61
	21	4		SAR	EXIZZZ	E 3		0443	C 069	AUG61
	22	7		MOW	BCXZZZ		X3	0447	M 733	AUG61
	23	7		ZA	0000		CFZZZZ	0454	C 000	377 AUG61
	24	7	ACRZZZ	ZA	0000		PFZZZZ	0461	E 000	367 AUG61
	25	7		SW	PFZZZZ-	7	CFZZZZ-	0468	E 360	370 AUG61
	26	7		ZA	KZRZZZ		REG	0475	E 861	357 AUG61
	27	7		MN	CPZZZZ		OPNZZZ	0482	D 577	874 AUG61
	28	7		B	MDVZZZ		CPNZZZ	0489	D 875	874 AUG61
	29	7		B	FFXZZZ		CPNZZZ	0497	D 982	874 AUG61
	30	7		MOW	KO7ZZZ		X1	0505	B 864	089 AUG61
	31	7		MOW	KO7ZZZ		X2	0512	M 864	094 AUG61
	32	7		ZA	PFZZZZ-	8	X3	0519	M 359	099 AUG61
	33	7		S	CFZZZZ-	8	X3	0526	S 369	099 AUG61
	34	7		BWZ	CBGZZZ		X3	0533	V 734	099 AUG61
	35	7		S	X3		X2	0541	S 099	094 AUG61
	36	7		BWZ	NOQZZZ		X2	0548	S 774	094 AUG61
	37	7		MZ	KZRZZZ		X2	0556	Y 861	094 AUG61
	38	7		ZA	PFZZZZ-	C	X3	0563	E 359	099 AUG61
	39	7		MZ	CFZZZZ		CFZZZZ-	0570	Y 377	3P0 AUG61
	40	7	OPZZZZ	ZA	CFZZZZ-	7 2	REG	0577	E 340	341 AUG61
	41	7		A	PFZZZZ-	7 2	REG	0584	E 340	341 AUG61
	42	7		MZ	REG	16	REG	0591	E 341	349 AUG61
	43	7		ZA	REG	16	REG	0598	Y 341	349 AUG61
	44	7		MOW	KZRZZZ	8		0598	E 349	AUG61
	45	7	CGMZZZ	B	INDZZZ		X1	0602	M 861	089 AUG61
	46	7	SIGZZZ	ZA	REG	- 24 1	REG	0609	B 808	313 0 AUG61
	47	7		MZ	REG	- 8	AC	0617	E 300	387 AUG61
	48	7		A	REG	- 8	AC	0624	Y 349	387 AUG61
	49	7		S	K1ZZZZ		X3	0631	A 857	099 AUG61
	50	7		B	X1		X3	0638	S 889	099 AUG61
	51	7		MOW	UNDZZZ	4	AC	0645	B 842	380 0 AUG61
	52	7		B	X3		AC	0653	M 099	379 AUG61
	53	7		BWZ	CVRZZZ		X3	0660	B 819	097 AUG61
	54	7	NCZZZ	BWZ	UNDZZZ		X3	0668	V 838	099 AUG61
	55	7		MZ	SKIZZZ		AC	0676	V 691	387 AUG61
	56	7	SKIZZZ	MZ	KZRZZZ		AC	0684	V 861	387 AUG61
	57	7	RESZZZ	MOW	KZRZZZ		AC	0691	Y 861	379 AUG61
	58	7		MOW	BOXZZZ		X3	0698	M 873	099 AUG61
	59	7		MOW	BOXZZZ-	3	X2	0705	M 870	094 AUG61
	60	7		MOW	BOXZZZ-	6 7	X1	0712	M 867	089 AUG61
	61	4		CH	PFZZZZ-	7	CFZZZZ-	0719	M 360	370 AUG61
	62	4		NOP	TRCZZZ			0726	N 794	AUG61
	63	4	FXIZZZ	B	COOC			0730	B 000	AUG61
	64	7	QBCZZZ	A	X3		X1	0734	A 099	089 AUG61
	65	7		BWZ	NOPZZZ		X1	0741	V 786	089 AUG61
	66	7		MZ	KZRZZZ		X1	0749	V 861	089 AUG61
	67	7		ZA	CFZZZZ-	8	X3	0756	E 369	099 AUG61
	68	7		MZ	PFZZZZ		PFZZZZ-	0763	E 367	380 AUG61
	69	7		B	CPZZZZ			0770	Y 577	AUG61
	70	7	NOZZZ	MOW	PFZZZZ		AC	0774	B 367	387 AUG61
	71	7		MOW				0781	M 367	AUG61



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PG	LIN	CT	LABEL	OP	A OPERAND	B OPERAND	D	LOC	INSTRUCTION	COMMENTS	PAGE 3	SC10
00	05	4		B	RESZZZ			1183	B 698	AUG61		
00	06	2	K17ZZZ	DCW	*			1189				
00	07	2	K24ZZZ	DCW	*			1191				
00	08	2	K51ZZZ	DCW	*			1193				
00	09	7	TRCZZZ	CS	0299			1194	/ 299			
00	10	7		MCH	CPZZZZ	C201		1198	M 577 201	AUG61		
00	11	7		SH	0203	C207		1205	M 203 207	AUG61		
00	12	7		MCH	ADRZZZZ 3	C205		1212	M 464 205	AUG61		
00	13	7		MCH	ADRZZZ- 4	C209		1219	M 457 209	AUG61		
00	14	7		MCH	PFZZZZ	C230		1226	M 367 230	AUG61		
00	15	7		B	RFCZZZ	CPZZZZ		1233	B 566 577 X	AUG61		
00	16	7		MCH	CFZZZZ	C251		1241	M 377 251	AUG61		
00	17	7	XXZZZZ	MCH	AC	C272		1246	M 387 272	AUG61		
00	18	7		MCH	EX1ZZZZ 3	C295		1255	M 733 295	AUG61		
00	19	7	RFCZZZ	MCH	EX1ZZZ			1262	M 2 730	AUG61		
00	20	7		B	REG	C282		1266	M 357 282	AUG61		
00	21	7	XXZZZZ	B	*XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	AUG61		1273	M 555	AUG61		
00	22	4	TRACON	SBR	*XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	AUG61		1277	H 591	AUG61		
00	23	4		MCH	EX1ZZZ 11	FX1ZZZ- 4		1281	M 730 726	AUG61		
00	24	4	TRCCFF	SBR	000C			1288	B 000	AUG61		
00	25	4		MCH	*XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	AUG61		1292	M 106	AUG61		
00	26	4	NZZZZZ	B	NZZZZZ 11	EX1ZZZ- 4		1296	M 107 726	AUG61		
00	27	4		DCW	C000			1303	B 000	AUG61		
00	28	1						1307		AUG61		
00	29				* THE PROGRAMMERS DECK -SPS- FOLLOWS							
00	30				* XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXALG61							
00	31				* THE FOLLOWING IS A PROGRAM DESIGNED TO							
00	32				* ILLUSTRATE THE USE OF SCION AND TO							
00	33				* CORRECTORATE THE OPERATION RESULTS SHOWN							
00	34				* ON PAGE 4 OF THE SCION WRITLUP.							
00	35				* N							
00	36				* T							
00	37	2	START	CC	OPCCDE	C209		1308	F 1			
00	38	7		MCH	AFLC	C226		1310	M W170 209			
00	39	7		MCH	RFLC	C247		1317	M W41 226			
00	40	7		MCH	ACFLD	C272		1324	M W48 247			
00	41	7		MCH	NSI	C295		1331	M W60 272			
00	42	1		CC				1338	M W34 295			
00	43	1		CC				1345	M T			
00	44	4		B	0295			1347	M 2			
00	45	4		B	TRACON			1348	M / 295			
00	46	4		B	SCICN			1352	B 577			
00	47	4		B	A			1356	B 388			
00	48	4		B	SCICN			1360	B V71 V81	*FADA	H	
00	49	4		B	A			1367	B 388			
00	50	4		B	SCICN			1371	B V71 V91	*FADA	C	
00	51	4		B	A			1378	B 388			
00	52	4	LABEL	B	AC			1382	B 387 W01	*FADAC	D	
00	53	4		B	SCICN			1389	B 388			
00	54	4		B	A			1393	B V81 V71	*FSBB	A	
00	55	4		B	SCICN			1400	B 388			
00	56	4		B	A			1404	B W11 387	*FSBC	AC	
00	57	4		B	SCICN			1411	B 388			
00	58	4		B	A			1415	B V81 V91	*FMPB	C	
00	59	4		B	SCICN			1422	B 388			
00	60	4		B	G			1426	B W11 W21	*FMPE	G	
00	61	4		B	SCICN			1433	B 388			
00	62	4		B	A			1437	B W31 387	*FMPF	AC	
00	63	4		B	SCICN			1444	B 388			
00	64	4		B	A			1448	B V91 V81	*FDVC	B	
00	65	4		B	SCICN - 4			1455	B 388			
00	66	4		B	A			1459	B W27 W21	*FDVF	G	
00	67	4		B	SCICN			1466	B 388			
00	68	4		B	F			1470	B W11 W31	*FDVE	F	
00	69	4		B	SCICN	1008		1477	B 388			
00	70	4		B	P			1481	B W21 W08	*FLTC	B	
00	71	4		B	P			1488	B 388			
00	72	4		B	X			1492	B V97 W03	*FLTD	3	
00	73	4		B	X			1499	B 388			
00	74	4		B	X			1503	B V91 W05	*FIXC	5	
00	75	4		B	X			1510	B 388			
00	76	4		B	X			1514	B W11 W20	*FIXE	20	
00	77	4		B	X			1521	B 388			
00	78	4		B	X			1525	B W11 W10	*FIXE	10	
00	79	4		B	X			1532	B 388			

IBM 1401-1403 PLANNING AND TESTING SHEET

PG	LIN	CT	LABEL	CP	A OPERAND	B OPERAND	D	LOC	INSTRUCTION	COMMENTS
2	101	7		X	G	1000		1536	X W21 #00	*FIXG U
3	110	4		B	SCICN			1543	B 388	
4	111	7		X	G	1000		1547	X W21 #00	*FXPG
5	120	4		B	TRCCFF			1554	B S92	
6	130	4		H	START			1558	• T08	
7	150	1C	A	DCW	*		511000000	1571		
8	160	1C	B	DC	*		509999999	1581		
9	170	1C	C	DC	*		503333333L	1591		
10	180	1C	D	DCW	*		5066666670	1601		
11	190	1C	E	DCW	*		555555555	1611		
12	200	1C	F	CC	*		9876543210	1621		
13	020	1C	G	CC	*		0000000000	1631		
14	030	3	NSI	DCW	*		NSI	1634		
15	050	7	AFLC	DCW	*		A-FIELD	1641		
16	050	7	BFLC	DCW	*		B-FIELD	1648		
17	051	12	ACFLD	DCW	*		AC-FIELD/REC	1660		
18	060	1C	OPCODE	DCW	*		CP A B	1670		
19	070									
20	080									
21	090									
22	090									
23	090									
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99	090									
100	090									

240 CARDS

\*NOTE SCICN CONTRCL CARD \*SCICN08TRACE\*  
 \*LCCATED AFTER PACKAGE DECK #1

/ T08 080

III. Object Sample Program Output / Sample Trace

DATA OBJECTS - PLANING AND TESTING FIELD

	P	A	B	A-FIELD	B-FIELD	AC-FIELD/REG	NSI
C	V71	V81		511000000E	509999991I	5119999999	
C	V71	V91		511000000E	50333333LL	5066666670	BT67
C	387	W01		506666667E	506666667-	0000000000	BT7P
E	V81	V71		509999991I	511000000E	441000000-	BT89
E	W11	387		555555555E	441000000-	5555555555	BUG0
E	V81	V91		509999999I	503333333L	503333333K	BU11
E	W11	W21		555555555E	987654321E	9999999999	BU22
E	W31	387		000000000E	999999999I	0000000000	BU33
E	V91	V81		503333333L	509999999I	503333333L	BU44
E	W27	W21		321000000E	987654321E	0000000000	BU55
E	W11	W31		555555555E	000000000E	9999999999	BU66
E	W21	*08		987654321E	000000000E	5855555598	BU77
P	V97	*05		000050666F	00004011E	5350666600	BU88
X	V91	*03		503333333L	000446402A	0000000000	BU99
X	W11	*20		555555555E		0000000000	BV1C
X	W11	*10		555555555E		5555555000	BV21
X	W21	*00		987654321E		0000000000	BV32
X	W21	*00		987654321E		0000000000	BV43
						0000000000	BV54



#### IV. Error Conditions

##### A. Overflow and Underflow

Two special conditions, peculiar to floating point arithmetic, known as Overflow and Underflow occur as a consequence of operations yielding answers that are not in the range of numbers prescribed for excess-50 floating point.

The overflow condition exists when a resultant characteristic is larger than 99. The SPS coding shown below indicates the manner in which this condition is detected and acted upon by the SCION subroutines ( the characteristic is accumulated in IR#3).

```
### ##### ##### #
B   OVR   X3 -2   1
### ##### ##### #
OVR NOP *+1
    MCW 9     AC
    MCW AC
    B   EXIT
### ##### ##### #
```

The point of the matter is that the SCION subroutines simply replace the AC-field with all nines when overflow is encountered. A normal exit is made and no other indication of the existence of overflow is given other than the contents of the AC-field.

##### B. Division by Zero

When an attempt is made to divide ( FDV ) by zero, SCION replaces the AC-field by all nines and proceeds to make a normal exit. This condition is detected within SCION by the first instruction in the divide ( DIVZZZ ) subroutine.

```
##### ### ##### ##### #
DIV   B   ALL9S  HIORB  0
##### ### ##### ##### #
```

One should note that the zero B-field determination is based on the presence of a zero in the high order position of the mantissa of the B-field. Actually the A-field address, ALL9S, is the label of the second instruction of the Overflow routine thereby maintaining the uniqueness of any special overflow procedure used.

The task of modifying the division-by-zero logic of SCION explained above is different than the procedure given for overflow and underflow. What is required is an overlay of the A-field address of the DIVZZZ instruction with the address of the routine programmed by the coder. It is important, however, that the programmer subsequently return to RESZZZ.

The important thing to observe about the SPS coding shown is that the first instruction of the OVR entry is a No-Operation code with the next instruction address in the A-field. Therefore, if the programmer finds it necessary to treat overflow in some special manner he has available to himself the ability to overlay the NOP instruction to effect one of three options:

1. Halt and proceed.
2. Halt and branch to a special routine.
3. Branch immediately to a special routine.

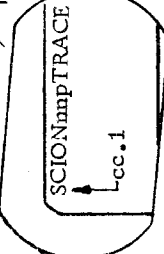
The last two options must be accompanied by a subsequent return to OVR+4 ( OVRZZZ+4 ) or to EXIT ( RESZZZ ) if further processing is desired.

The Underflow condition is somewhat similar to the Overflow logic except that is detected by finding the resultant characteristic ( IR#3 ) to be negative; whereupon, the AC field is replaced by all zeros and normal exit is made.

Again, the first instruction of this error condition entry ( UNDZZZ ) is a NOP type instruction. Hence, the same modification procedures as were explained for overflow are applicable for the special treatment of the underflow condition

V. Using The System  
A. Operating Procedures

KEYS/LIGHTS Sequence		1402 Card Sequencing					
1401	1402	Read Hopper	Read Stacker Normal	Read Stacker #1	Punch Stacker Normal	Punch Stacker #4	1403
depress RESET CHECK and START RESET	depress RESET CHECK and LOAD	<ol style="list-style-type: none"> <li>1. SCION II, Part 1 (first 17 cards)</li> <li>2. Control Card</li> <li>3. SCION II, Part 2</li> <li>4. SPS Source Deck (with macros)</li> <li>5. blank cards</li> </ol>					
				<ol style="list-style-type: none"> <li>1. Control Card</li> </ol>			
			<ol style="list-style-type: none"> <li>1. SCION II, Part 1</li> <li>2. SCION II, Part 2</li> </ol>	<ol style="list-style-type: none"> <li>2. SPS Source Deck (with macros)</li> </ol>	<ol style="list-style-type: none"> <li>1. SPS SOURCE with LINKAGES</li> </ol>	<ol style="list-style-type: none"> <li>1. SCION routines, with ORG 333</li> </ol>	SPS Listing of Punch Stk. Norm.



where: nn is the mantissa size desired, eg. 08  
p designates the subroutines desired  
TRACE is punched if tracing is desired.

\* The SPS system utilized will determine the ordering of the decks required, if any.

## V. B. Restrictions and Precautions

Index registers #1, #2, #3 are utilized by SCION. Upon assembly of the total program the subroutines will have defined these index registers by DCW's designating each as a three position field. Within the subroutines these index registers are used as accumulators, therefore, it is imperative that no other word marks be entered into these fields or that the high order word mark be removed at entry time. If the index registers are used in their normal manner this should of little concern to the programmer, because the SCION routine preserves the contents of these registers.

The first card produced for the stipulated SCION subroutines will always be an ORG 0333. However, if the programmer desires to map the subroutines some other place in memory he has this opportunity to change the ORG card before SPS assembly. In this event, there does exist one restriction that the work areas of the subroutines not be located in memory above 3999. This restriction is a result index register logic peculiar to memory above 3999.

Instruction modification using the SPS device of character adjustment relative to the executing instruction ( eg - MCW \*-5 ) should be utilized with discretion for the two following reasons:

1. Subsequent patching
2. Macro instructions are actually eleven characters in length, but appear to be seven characters at the SPS level.

An example of erroneous coding is:

```
### ##### #####
MCW ADRES * +14
FAD TANGT ANGLE
MCW AC 0000
```

One correct method would be:

```
### ##### #####
MCW ADRES LBL +6
FAD TANGT ANGLE
LBL MCW AC 0000
```



CLEAR STORAGE 1  
 CLEAR STORAGE 2  
 FOOTSTRAP CARD

,00E015,022026,C30034,C41,045,053,0570731026  
 L072116,11C108,105117B1C17T99,027A07402E027B0C10270B026/0991,001/00111710  
 ,00F015,022029,C560637,056629 ,02406671056

FD	LN	CT	LABEL	OP	A OPERAND	B OPERAND	L	LOC	INSTRUCTION	COMMENTS
				CTL	31					
					* THIS IS DECK#3- CREATES SCION LINKAGES FOR SPS					
10	C1C			CRG	0333					
11	C2C			SW	0001	C101				AUG61
12	C30	7	DECK3	S	SEC			0333	001	101
13	C4C	4		CC	READ			0340	S 974	
14	C50	5	SKIP					0344	F 762	1
15	C6C				*XXAUG61					AUG61
16	C70	4	MACRO	CS	0139			0349	/	139
17	C80	7		MCH	C251			0353	/	251
18	C90	7		MCH	C013	C113		0357	M	013
19	100	7		MCH	C202	C211		0364	M	202
20	110	7		MCH	0005	C206		0371	M	005
21	120	7		MCH	0013	C216		0378	M	013
22	130	7		MCH	BSCICN	C122		0385	M	932
23	140	7		MCH	C222	C101		0392	M	222
24	150	7		MCH	BSCICN	C227		0399	M	932
25	160	7		MCH	BSCICN-	B	C218	0406	M	924
26	170	1		FP				0413	G	
27	180	4		CS	0267			0414	/	267
28	190	8		B	FO			0418	B	433
29	200	7		A	KT	C004		0426	A	923
30	C1C		FC	MCH	0105	C105		0433	M	105
31	C2C	4		SW	0252	C206		0440	M	252
32	C30	7		MCH	0257	C113		0444	M	257
33	C4C	4		MCH	0030	C267		0451	D	038
34	C50	7		MCH	0032			0458	D	032
35	C60	4		MCH	0027	C261		0462	D	027
36	C70	7		MCH	0021			0469	M	021
37	C80	7		MCH	0016			0473	M	016
38	C90	7		MCH	ASTER	C255		0480	M	963
39	100	7		MCH	0267	C255		0487	M	267
40	110	7		MCH	0236	C236		0494	M	222
41	120	7		MCH	0037	C245		0501	M	245
42	130	7		MCH	0026	C231		0508	M	026
43	140	7		MCH	0245	C137		0515	M	231
44	150	7		MCH	0231	C126		0522	M	231
45	160	7		MCH	0038	C138		0529	D	038
46	170	7		MCH	0027	C127		0536	D	027
47	180	7		MCH	TA	C015		0543	B	684
48	190	7		MCH	FS	C015		0551	B	702
49	200	7		MCH	FM	C015		0559	B	720
50	010	7		MCH	FL	C015		0567	B	738
51	020	7		MCH	FL	C015		0575	B	616
52	030	7		MCH	ERRFLT	C267		0583	B	598
53	040	7	FI	MCH	FIX	C220		0591	M	962
54	050	7		MCH	FIX	C116		0605	M	944
55	060	7		MCH	FLT FIX			0612	B	630
56	070	7	FL	MCH	FLT	C220		0616	M	947
57	080	7	FLT FIX	MCH	FLT	C116		0623	M	947
58	090	7		MCH	ZA	0236		0630	E	236
59	100	7		MCH	F1	C237		0637	B	652
60	110	7	FI	MCH	THOLSN	DEC		0645	E	237
61	120	7		MCH	FZ	C239		0652	M	969
62	130	7		MCH	DEC	C138		0659	Y	964
63	140	7		MCH	DEC	C239		0666	A	965
64	150	7		MCH	0239	0131		0673	M	239
65	160	7	FA	MCH	F2			0680	B	752
66	170	7		MCH	FAD	C116		0684	M	941
67	180	7		MCH	FAD	C220		0691	M	941
68	190	7	FS	MCH	F2			0698	B	752
69	200	7		MCH	FSB	C116		0702	M	938
70	C1C			MCH	FSB	C220		0709	M	938
71	C2C			MCH	F2			0716	B	752
72	C30			MCH	TMP	C116		0720	M	935
73	C4C			MCH	TMP	C220		0727	M	235
74	C50			MCH	F2			0734	B	752
75	C60			MCH	FDV	C116		0738	M	950
76	C70			MCH	FDV	C220		0745	M	950
77				FP				0752	6	

PC	LIN	CT	LABEL	OP	A OPERAND	B OPERAND	C	LOC	INSTRUCTION	COMMENTS	UCK
13	08C	4		CS	0267			0753	/ 267		
13	C90	5		B	SKIP			0757	B 344		
13	100		REAC	R				0762	I		
13	110	2		SS				0763	K I		
13	120			S	0005	SEQ		0765	S 005	274	
13	130	8		BWZ	F3	0201		0772	V 787	201	X
13	140	7		MCH	ASTER			0780	M 963	201	
13	150	7	F3	ZA	0005	SEQ		0787	E 005	274	
13	160	7		MCH	0055	0155		0794	M 055	155	
13	170	7		MCH	0055	0267		0801	M 055	267	
13	180	8		B	F2	0008		0808	D 752	008	*
13	190	8		B	MACRO	0014		0816	B 349	014	F
13	200	7		CS	0251			0824	/ 251		
14	010	7		SW	0249			0828	/ 249	236	
14	C20	7		SW	0222	0236		0835	/ 222	218	
14	030	7		SW	0211	0218		0842	/ 211	208	
14	C40	7		SW	0202	0208		0849	/ 202	201	
14	050	7		MCH	0039	0201		0856	M 039	249	
14	060	7		MCH	0038	0249		0863	D 038	247	
14	070	7		MCH	0037	0245		0870	M 037	245	
14	C80	7		MCH	0027	0233		0877	M 027	233	
14	090	7		MCH	0026	0231		0884	M 026	231	
14	100	7		MCH	0016	0220		0891	M 016	220	
14	110	7		MCH	0013	0216		0898	M 013	216	
14	120	7		MCH	0007	0209		0905	M 007	209	
14	130	7		MCH	0005	0206		0912	M 005	206	
14	140	4		B	F2			0919	B 752		
14	150		K1	DCH	*			0923	I		
14	160	9	BSCION	DCH	*			0932	B SCION		
14	170	3	FMP	DCH	*			0935	M		
14	180	3	FAC	DCH	*			0938	ZS		
14	190	3	FIX	DCH	*			0941	ZA		
14	200	3	FLT	DCH	*			0944	X		
14	020	3	FLV	DCH	*			0947	P		
14	030	3	ERRFLT	DCH	*			0950	D		
14	040	3	ASTER	DCH	*			0962	*OP CODE ERR		
14	050	2	DEC	DCH	*			0963	*		
14	060	2	TFCUSN	DCH	*			0965			
14	070	5	SEC	DCH	*			0969	1000		
14	C80			DCH	*			0974			
14	C90			DCH	*			0974			

\* THIS DECK IS FOLLOWED BY THE SPS SOURCE PROGRAM

7 333 080

112 CARDS