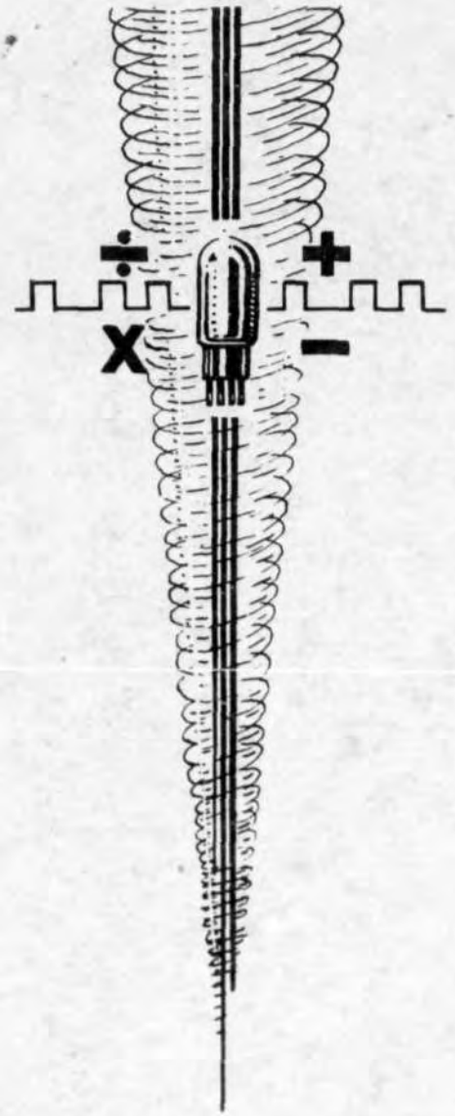

PROJECT WHIRLWIND

Contract N5ori60

INITIAL TESTING OF A COMPUTER ELECTROSTATIC STORAGE SYSTEM

APRIL 23, 1951

SERVOMECHANISMS LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Copy 5

PROJECT WHIRLWIND

Report R-195

INITIAL TESTING OF A COMPUTER ELECTROSTATIC STORAGE SYSTEM

Submitted to the
OFFICE OF NAVAL RESEARCH
Under Contract N5ori60
Project NR-048-097

Report by
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Project DIC 6345

April 23, 1951
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FOREWORD

Following preliminary tests of the individual Whirlwind electrostatic-storage tubes, 16 tubes were installed in a bank in the Whirlwind computer. This thesis report describes the initial testing of the bank as a system, first without and then with the main control circuits of the computer. Because it has had only limited distribution, it is being issued as a Project Whirlwind R-series report.

The author wishes to express his sincere appreciation to Mr. Jay W. Forrester, head of Project Whirlwind, for the use of the library and laboratory facilities of the Project, to Mr. Patrick Youtz for his careful supervision of the thesis, and to Mr. Stephen Dodd for his generous aid and advice concerning the technical details of the work. The author acknowledges also the work of the Project Whirlwind staff in the design of the systems with which much of the thesis is concerned.

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ABSTRACT

The use of the M. I. T. Electrostatic Storage tubes in the Whirlwind I computer required initial tests to determine suitable operating conditions for the tubes, tolerances on the conditions, and a measure of the reliability of the control circuits and driving circuits.

The first tests on the system were conducted without the flexibility of the main control circuits of the computer; the tests were restricted to cycling various arrays over the 256-spot arrays. The usefulness of a number of patterns was investigated, and the most useful appeared to be two complementary patterns. They did not result in long-term reliable operation of the storage system, however, and tests were discontinued when the main control circuits became available. The cycling tests were used very effectively to study reliability of the driving circuits, and in a few cases, to improve their design. The control circuits were checked by a built-in, simulation type check. When the storage system was incorporated with the rest of the computer, the driving circuits and control circuits had been eliminated as sources of errors of significant frequency.

The cycling tests gave evidence of three important weaknesses in the ES system:

1) Deflection drift,
2) Need for different writing grid drives for write-plus and write-minus,
3) Interaction.

The most significant of these was the deflection drift. The most important source appeared to be in the walls of the storage tube, where bare

portions of glass were being charged sufficiently to deflect the beam. The weakness has resulted in a tube design, not tested in the system which eliminates the opportunity for glass to charge. In the final phase of the tests, the fault was cured to some extent by increasing the spot size, with resulting increase in the interaction.

The inability to completely erase a suitable positive spot with a write-minus of the same grid-drive led to redesign of the driving circuits to provide separate drives for write-plus and write-minus. The diameter of the writing beam is proportional to grid-drive at least in the useful region. The facility of separate writing gates provided a significant increase in reliability, since any size of a positive spot could be erased.

The principal characteristics of interaction -- the effect on adjacent areas of the use of the high-velocity gun on a spot -- were measured independently of the cycling tests. However, it was a source of errors in the cycling tests, and became more troublesome in the final phase of the initial tests. The requirement of large spots, and the necessarily large erasing currents, made interaction very severe. It was corrected by adding holding-gun time to each operation at the expense of ES operation time.

The elimination of deflection drift has been the goal of recent modifications in the storage tube design. It should be significant in increasing the efficiency of the storage system by eliminating the extra holding-gun time necessary to combat interaction, and provide a much greater degree of reliability.

CHAPTER I

INTRODUCTION AND STATEMENT OF THE PROBLEM

1.1 Introduction

The requirement of a high-speed storage element to serve as the memory of an electronic, digital computer* has led to the development and construction of an electrostatic storage tube[1] by the laboratories of Project Whirlwind, Servomechanisms Laboratory, at M. I. T. The computer is a parallel machine which operates at a basic clock-pulse frequency of 1 megacycle. Information is transferred to or from storage at 5 to 16 microsecond intervals disregarding the time spent in the use of the storage element itself. The storage operations are intended eventually to be performed in about 6 microseconds in order to be in balance with the operating speeds of the rest of the machine. Eventually, each storage tube will store 1024 positive and negative electron charges or "spots", which are the coded orders and numbers comprising the programs.

The storage element is a parallel system as are the rest of the internal elements of the computer. That is, the 16 storage tubes, each corresponding to a digit of the orders and numbers involved, receive or write information simultaneously and deliver or "read" information simultaneously. In the indefinite interval between writing and reading, the data in the tubes are stored and maintained at their stable states, so that they are available to be read at any time. Although the storage surface itself is round, the positions occupied by the useful data on the surface form a square array of discrete spots; eventually the surface will have 32 spots on each side. At the stage of initial tests, however, the goal of a useable 16 x 16 spot array was

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* Glossary: A.1

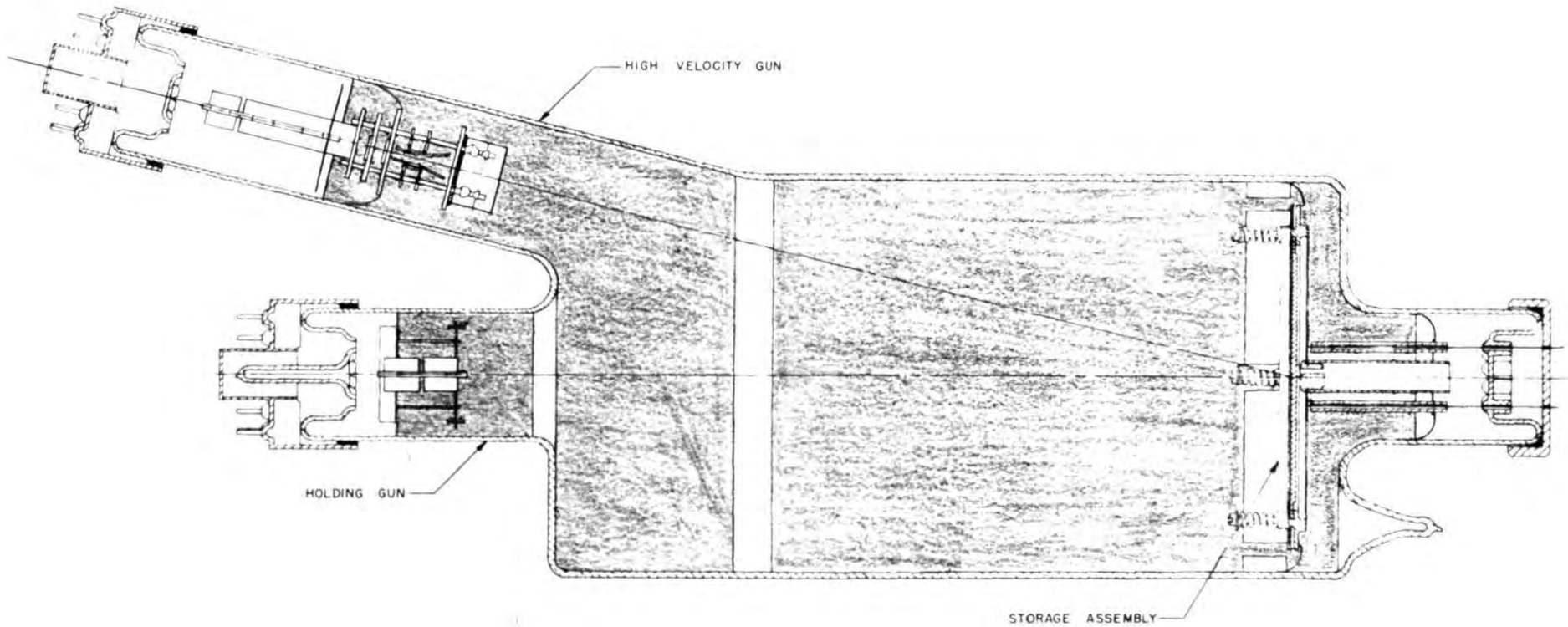
1. Superscripts refer to references in the bibliography.

sought.

1.2 Operation of the Storage Tube

The ability of a device to store binary information requires that two stable states be present in its operation. It is also desirable that they be continuously stabilized in order to avoid regenerating the information stored. The Whirlwind I storage tube (figures 1 and 2) utilizes the phenomenon of secondary emission to establish the charged areas at the stable potentials on the storage surface, to sense the condition of the stored charges, and to maintain or hold the stable conditions continuously as long as power is supplied.

In the storage tube, the storage surface is a material which, when bombarded by electrons, has a secondary emission ratio δ which varies from 0 to about 3 depending on the velocity of the primary electrons (figure 3.) The emission velocity of the secondary electrons is low except for a small percentage approximately at the velocity of the primary electrons. By locating a collector grid adjacent to the surface, the secondary electrons will be attracted to the collector or repelled back to the surface depending upon whether the collector is at a higher or a lower potential than the surface. Since the surface is an insulator, it will be charged in a direction which depends on the collector potential and on the secondary emission ratio corresponding to the velocity of the primary electrons. If the secondary emission ratio δ is greater than unity the net electron current may be either toward or away from the surface and the surface will charge toward the potential of the collector. If, however, δ is less than unity the surface will charge negatively toward a potential near the cathode, as long as δ remains less than 1. By directing a narrow beam of electrons whose velocity is between



STORAGE TUBE ASSEMBLY
SECTIONAL VIEW

FIG. 1

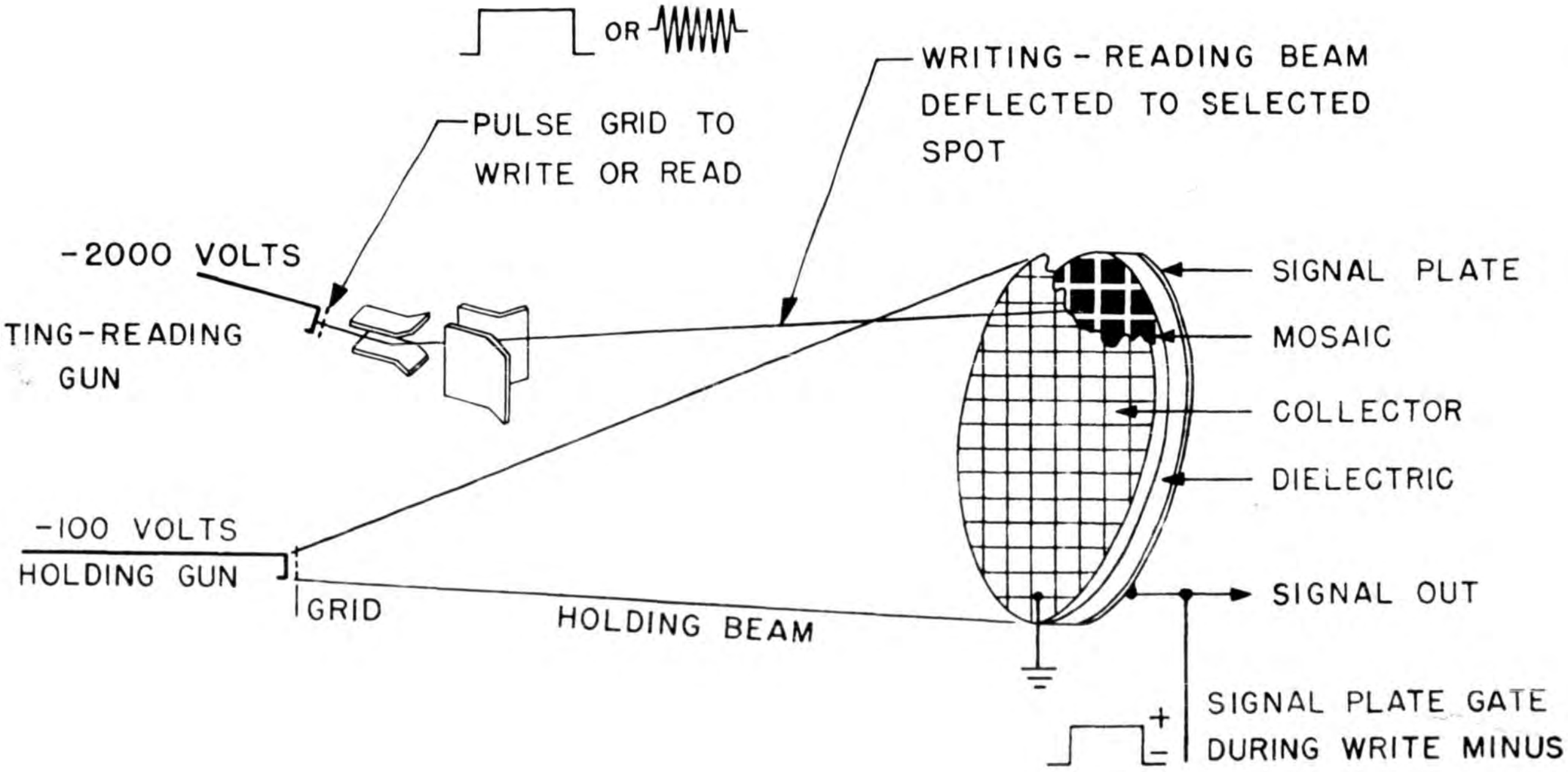


FIG. 2

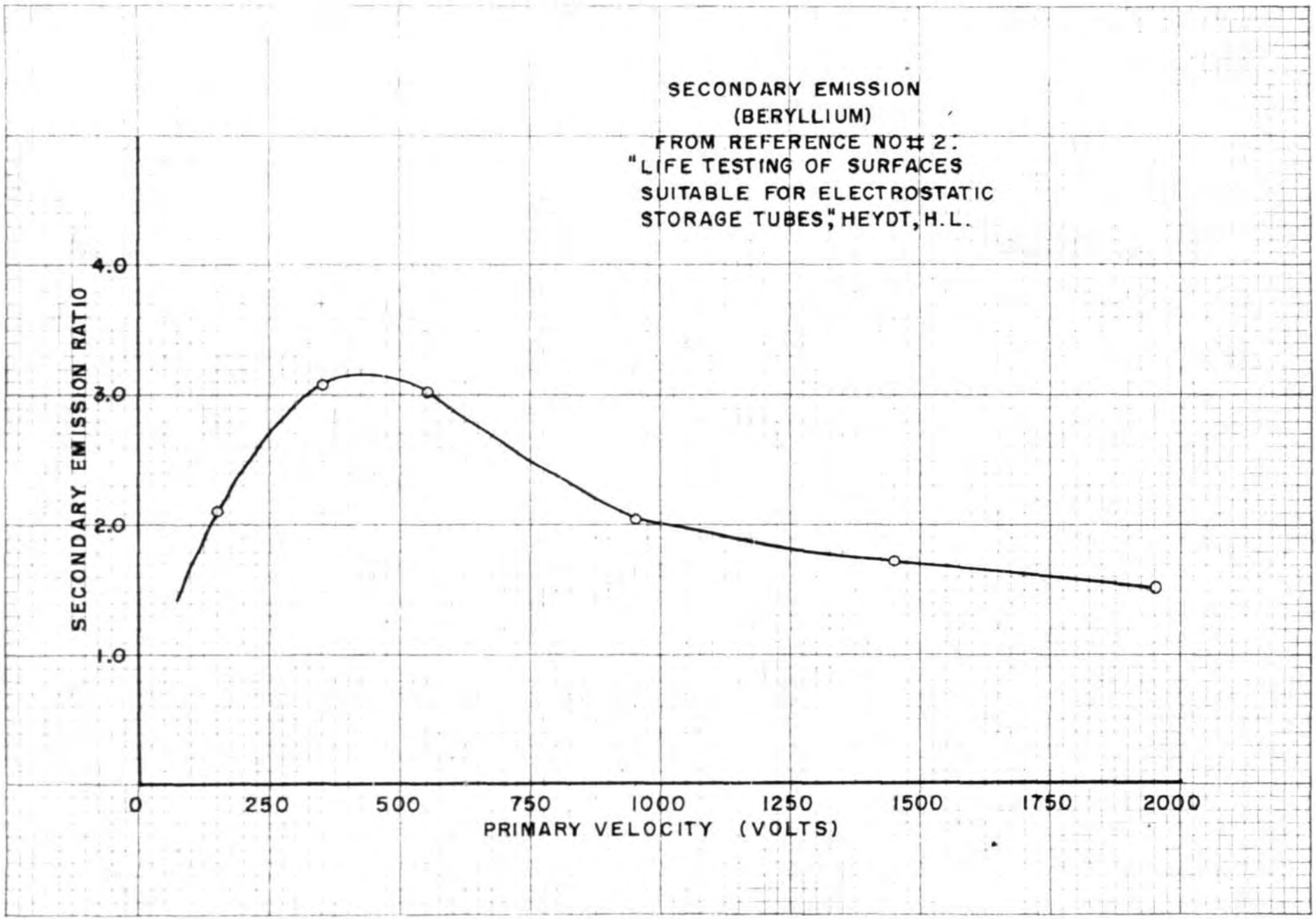


FIG. 3

first and second crossover ($\delta > 1$) at a spot on the surface, the spot will be charged to the potential of the collector. In order to charge a spot to a lower potential, the potential of the entire surface is raised, during the time the high-velocity beam is on, by an amount approximately equal to collector-to-holding gun cathode voltage. The high velocity electrons charge the spot to collector potential, and after the surface is lowered to its original condition the spot will be negative with respect to the collector. The surface is raised or switched to the higher potential by applying a gate* to the signal plate.

After writing the spots at either the collector or holding-gun cathode potential, it is necessary to supply it with a stream of electrons which will hold the spot at the desired potential. A constant source of low-velocity electrons is provided to spray the entire surface; the source is turned off during writing and reading, and is called the holding gun. The stable conditions of the spots under its action are at holding-gun cathode and collector potentials. The net current to a spot on the surface for various values of spot potential is shown in figure 4; the value at which δ is unity is called first-crossover. It is about 20 volts for these tubes. As long as the stabilising (electron) current is negative to a given spot, the spot will be charged negatively until it reaches the nearest stable potential. If, on the other hand, the stabilising current is positive, the spot will charge in a positive direction until it reaches the nearest equilibrium point. Consequently, any tendency for a spot to change its potential due to leakage or redistribution of secondaries due to operations on neighboring spots will be counteracted by the action of the holding beam. If a sufficiently long holding-gun time were available, it would be necessary only to write a spot to a potential above that of first-crossover if the spot were to be positive

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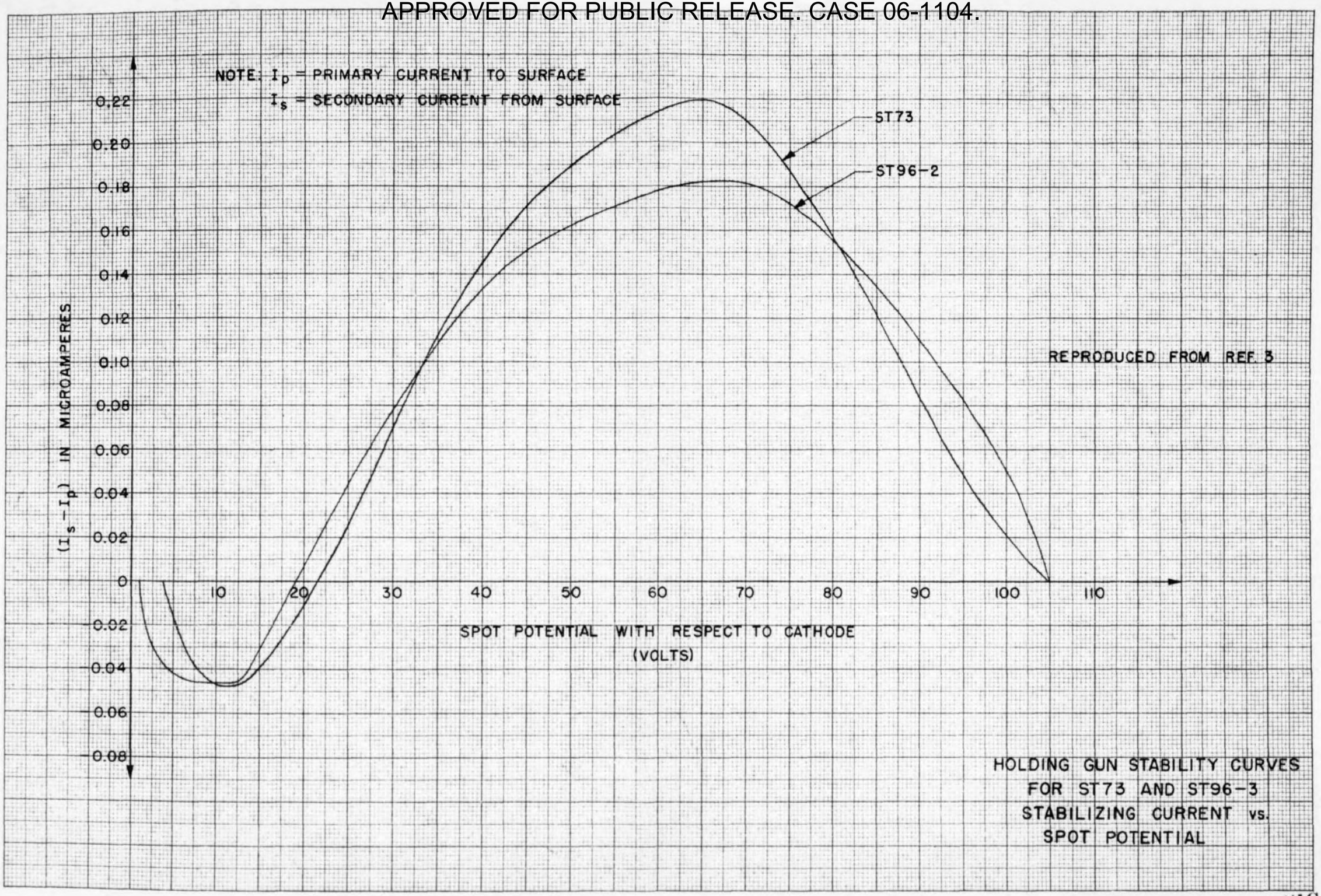
* Glossary: A.2



HOLDING GUN STABILITY CURVES
FOR ST73 AND ST96-3
STABILIZING CURRENT vs.
SPOT POTENTIAL

FIG. 4

or below first-crossover if the spot were to be negative. In order to minimize the time required to stabilize a spot at the desired potential, it is necessary to write the spot as near to the stable points as possible. Otherwise, the spot may not be at its proper voltage when a subsequent reading occurs.

The binary information stored as positive or negative spots can be read by a process similar to writing. In order to distinguish between the two polarities of spots, the surface potential is raised by an amount about equal to first-crossover to collector voltage. The high-velocity gun is turned on, and since the value for δ is greater than 1, the spot under the beam will be charged toward collector potential. The electron current to the spot is negative or positive depending on the potential of the spot. The charging current develops a signal across the signal-plate to ground impedance. In order to discriminate between the signal and the gates applied to the signal plate, the high-velocity beam is modulated by a 10 m.c. r-f signal and the signal-plate impedance is a tuned circuit. A wide-band output amplifier brings the 100 microvolt output signal to a level of about 15 volts, and a phase-sensitive circuit detects the polarity of the output signal. This signal is applied to the suppressor grid of a gate tube and a sensing pulse is simultaneously applied to the control grid. A positive spot is detected as the presence simultaneously of the positive output signal and the sense pulse, developing a signal at the plate of the gate tube. A negative output pulse maintains the gate tube in its cut-off state.

In order to familiarize the reader with the operation of the storage tube, it will be helpful to discuss briefly the most basic method of determining the condition of the storage-surface. If an area on the storage-surface is at the negative stability potential, it can be charged positive about 20 volts

before entering the positive restoring region of the holding-gun current and switching positive. The high-velocity beam can be used to charge a negative area toward collector voltage without switching the area, as long as the net charge transferred to the area is less than that required to switch the area above first-crossover. It has no effect on the stability of positive areas, because they are stable at collector voltage. The high-velocity beam can be swept rapidly over the surface, producing charging currents from negative areas at the signal plate, without basically changing the condition of the surface; the holding beam will constantly restore negative spots back to their stable voltages. By modulating the high-velocity beam with RF, a suitable output signal is produced from the negative areas, and a null from the positive areas. The output signals, taken directly from the output of the phase-detector, are used to intensity modulate the beam of a cathode-ray tube. By applying the same sweep voltages to the display tube as to the storage tube, the charge condition of the surface can be observed on what is called the "TV display."

1.3 Scope of Initial Tests

1.31 Tests Accomplished Preliminary to Installation in Whirlwind

All storage tubes, prior to being installed in Whirlwind, were subjected to two types of tests. The first of these was the production test; it was primarily intended to eliminate those tubes which did not conform to the specifications for assembly and processing. The results of the tests described as well as possible from static tests the gas content, the transfer characteristics of the guns, the deflection sensitivity and relative positioning of the high velocity guns, the action of the holding gun on the surface, and the limits of stability of the surface under holding-gun action.

The second class of tests was concerned with the dynamic characteristics of the tubes. The test was intended to: 1) determine the desirable range of the voltages applied to the tube, such as focus, collector to HG-cathode

voltage and high-velocity gun bias; and, 2) determine the amplitudes and allowable duration of the gates applied to the high-velocity and holding-gun grids and to the signal plate. These tests[4] were performed in the Storage Tube Reliability Tester, which was designed to simulate to as great an extent as possible the conditions expected in the computer without the elaborate control and intermediate storage facilities provided by the computer. From these tests, it was intended that the suitability of each tube for the computer be determined, as well as a useful set of operating characteristics.

1.32 Goal of Tests

The ultimate goal of the initial tests was to establish the storage system in a state of reliable operation. This goal included the valuable factors of validating and, if necessary, improving the design of the circuits in the system and determining the parameters in the storage tubes necessary for their reliable operation. In order that the tests not slow down the final tests of the arithmetic and control elements of the computer, it was necessary to simulate these elements by means of a test control. Since the operating mode during testing was of necessity different than the expected operating mode in the computer, so much so as to render the results of such tests to some extent indefinite, a final phase of the test was to tie the storage system in to the computer and observe the results. On that basis, the ultimate goal was not sought directly. However, the test control was to be sufficiently flexible to thoroughly test the storage tube control circuits, and to learn enough of the operation of the storage tubes in the system to make any required changes in their operating conditions a problem that could be met by using familiar procedures.

1.33 Systems Testing

The course followed in the initial tests was that of a systems test. The operating conditions determined in the early dynamic tests were used as

a starting point and to this extent the operation of the storage was assumed to be satisfactory.

The output signals from the storage tube, both dynamic and static, were used as the criterion of their operation.

Any improper operation was generally followed by further testing to provide sufficient symptoms to isolate the source of the failure. Although sometimes the trouble location led eventually to the investigation of a circuit in the system, such an investigation was not conducted separately as a goal in itself. It is for this reason that the tests must be called systems tests. Basically, they included testing of the circuits from a functional point of view, or as they contributed to the overall desired result.

Quite exhaustive tests had been conducted on the storage tubes prior to their installation in the system. Although the results of these tests proved finally to provide only a first approximation to a suitable set of operating conditions, the tubes were initially considered to be "known" elements of the system. Very few basic investigations of their characteristics were conducted in the system for this reason. The emphasis was on optimizing the initial conditions, and investigating principally those factors which were common to all tubes, such as writing and rewriting times.

This approach almost immediately signified the need for organized procedures of investigating faulty conditions, essentially trouble location procedures. Although primarily directed toward maintaining the degree of reliability which had been achieved as the tests progressed, the procedures were also intended to be of value in the later testing and maintenance routines. The emphasis here was toward finding a variety of problems to adequately test the system, once the initial tests had been completed. Such procedures, in order to be valid at the high speeds required of the system, were of necessity self-checking. Having found the weaknesses of the system and having minimized

them, the test problems must be designed to aid in measuring the existing margin of operation, particularly of the weak elements. Here again, in order that the tests be performed efficiently, it was desirable that they be functional tests of the system.

Although the significance of the tests preliminary to the installation of circuits and storage tubes in the system has not been mentioned, it must not be overlooked. Usually, since they are not goals in themselves, such tests do not assume much prominence. With regard to the repetitive elements -- the driver circuits of the system -- this fact is still applicable. However, the storage tubes themselves are repetitive elements only functionally. Their operating conditions were expected to vary enough to warrant testing individually as was done in the preliminary tests. It was on this account important to validate the results of the preliminary tests by the initial systems tests. Because the whole system could not reasonably be tied up for testing a replacement tube, for instance, the preliminary tests must be evaluated in the light of experience in the system.

1.34 Important Factors in the Tests

A few singularly important factors in the operation of the system can be mentioned as goals of test procedures. The first of these is timing. It is concerned with the duration of the gates used, and with the times at which interdependent gates or pulses occur. An example of the timing problem is the requirement that the sensing pulse at each output gate occurs near the maximum amplitude of the readout gating pulse from the storage tube. Another example lies in the timing of the high-velocity gun gate with respect to the signal-plate gate during a write-minus operation; if the high-velocity gun is still on while the signal-plate gate is being removed, the spot under the beam will charge positively, making a write-minus operation less effective. All gate-generators in the system are standard flip-flops, with buffer amplifiers

added, except for the RF reading pulse-generator. The latter is a one-shot multivibrator of controllable duration. Except for this element, the duration of the gates is determined by "on" and "off" pulses which originate in the control section. Consequently, the timing can be expected to be as stable as the elements which provide the timing pulses.

The second important factor which can be expected during the tests is deterioration, particularly of the timing control and driving circuits. The deterioration of the storage tube guns will be measured starting with the results of the initial tests, hence will not be considered in detail here. Deterioration of the timing control circuits will produce results which have two important characteristics. First, the interval between the timing pulses will be in error; if the failure is intermittent, as is often expected of early failures, the effect will be a change in the charge condition of the storage surfaces to an extent that may or may not produce an error in the data stored. The second characteristic is that the failures will produce symptoms which are similar in all storage tubes. Errors common to all tubes can generally be traced to control failures, although all control failures may not be serious enough to produce symptoms identifying the failures. An automatic method of checking control is required. Errors which occur in the storage tube driving circuits will lack this distinction. The failures of gate-generators can probably be eliminated by familiar maintenance procedures.[5] It is important to discover the more common types of circuit failures to facilitate these procedures. A more troublesome fault is expected to be the diminishing of gate amplitudes due to deterioration in their amplifiers. The most obvious method, the direct measurement of the amplitudes as a routine maintenance step, is so cumbersome as to make it unreasonable for anything but the earliest tests.

The third factor is the repetition frequency in the system. With

regard to the circuits, the generated gates and other pulses must be without substantial variations in time, duration, and amplitude over a wide range of frequencies. The storage system must operate at nearly zero frequency at the lower limit, and at about 40 microsecond intervals for the upper limit. The timing of the control pulses is dependent on circuits which have, for the most part, been thoroughly investigated in this respect and pose a distinct reliability problem.

The sensitivity of the gate amplitudes to frequency has been investigated in production tests by observing the lower, upper, and a few middle repetition rates. Since the effects of this factor are interdependent with gate stability, a test for one should be made to test for the other.

With regard to the storage tube itself, the problem of sensitivity to repetition frequency is very complex. Considering it as a bistable element, the restoring time under holding-gun action of an area toward its stable state (figure 5) is very long with respect to the writing times, which are in the order of 20 microseconds. Consequently, it is necessary to control all factors which lead to deterioration or instability as much as possible. The effect of the charging of spots, particularly negative spots, under the read beam, for instance, must be overcome by rewriting the original contents immediately after it is read out. The signal-plate gate must be set to write any spot reliably below first-crossover without writing it below holding-gun cathode voltage; if the latter occurs, an ensuing write-plus operation will be less effective. The writing times must be set with respect for the interaction that writing produces on adjacent spots. The problem of setting up the storage tubes themselves resolves itself into achieving a standard routine which is sufficiently flexible to be adaptable to tubes of varying gun and stability characteristics.

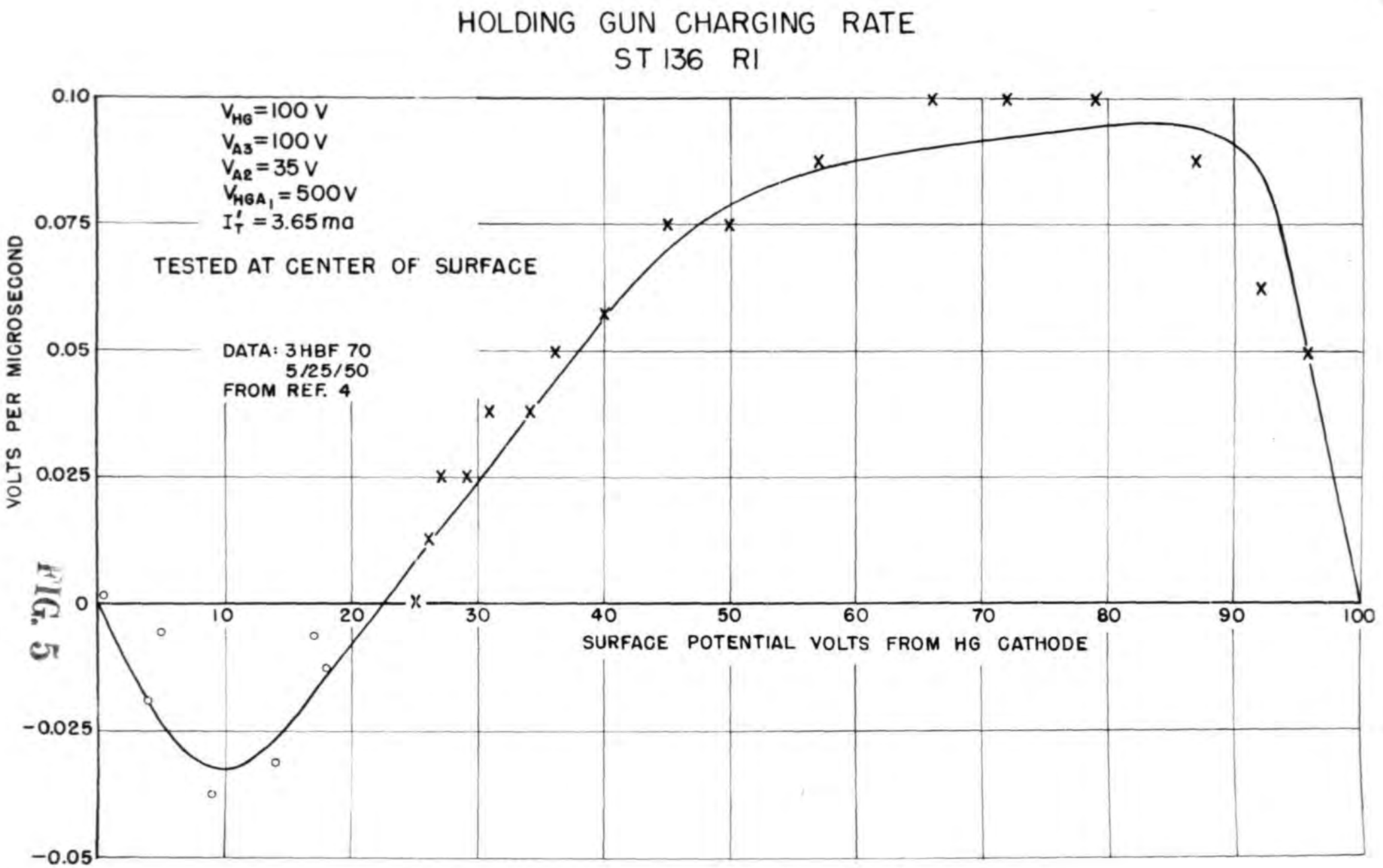


FIG. 5

CHAPTER II

THE INITIAL ES SYSTEM

2.1 The Storage Tube and Driving Circuits

The circuits used with each storage tube in the read and write operations are shown in block schematic form in figure 6. The flip-flop shown (FF1) provides for temporary storage of the information to be written. At the start of each write or rewrite cycle, t_1, it is sensed. If a "0" is to be written the high-velocity gun gate in the corresponding ES driving circuit is initiated, and a signal-plate gate is applied for the duration of the writing gate. At the end of the writing operation, the spot is in the negative restoring region, and will restore to the negative stable potential. The high-velocity gun gate generators in all digit columns are initiated at a later time, t_2. In those digits where a "0" is being written, the gates are already on, and the initiate pulse at t_2 has no effect. In those digits where no write-minus is occurring, turning the guns on effects a write-plus. The convention that "0's" correspond to negative spots and "1's" to positive spots is thus established. All writing gates are terminated simultaneously at t_3. During the read operation, the write-read gun is driven by a 1.5 microsecond pulse of 10 megacycle r.f., simultaneously with switching the signal plate by a small voltage; the beam current charges the spot toward collector potential, the direction of the signal-plate current being dependent on the direction in which the spot charges. After being detected, the output signal is used to control a gate tube. Only the "1" outputs (from positive spots) are used. A positive output signal allows the sense pulse to emerge and set the intermediate storage flip-flop to a "1". The flip-flop shown is used both in reading and in writing. Since the flip-flop holds the information from storage immediately after a read, the rewrite can be initiated

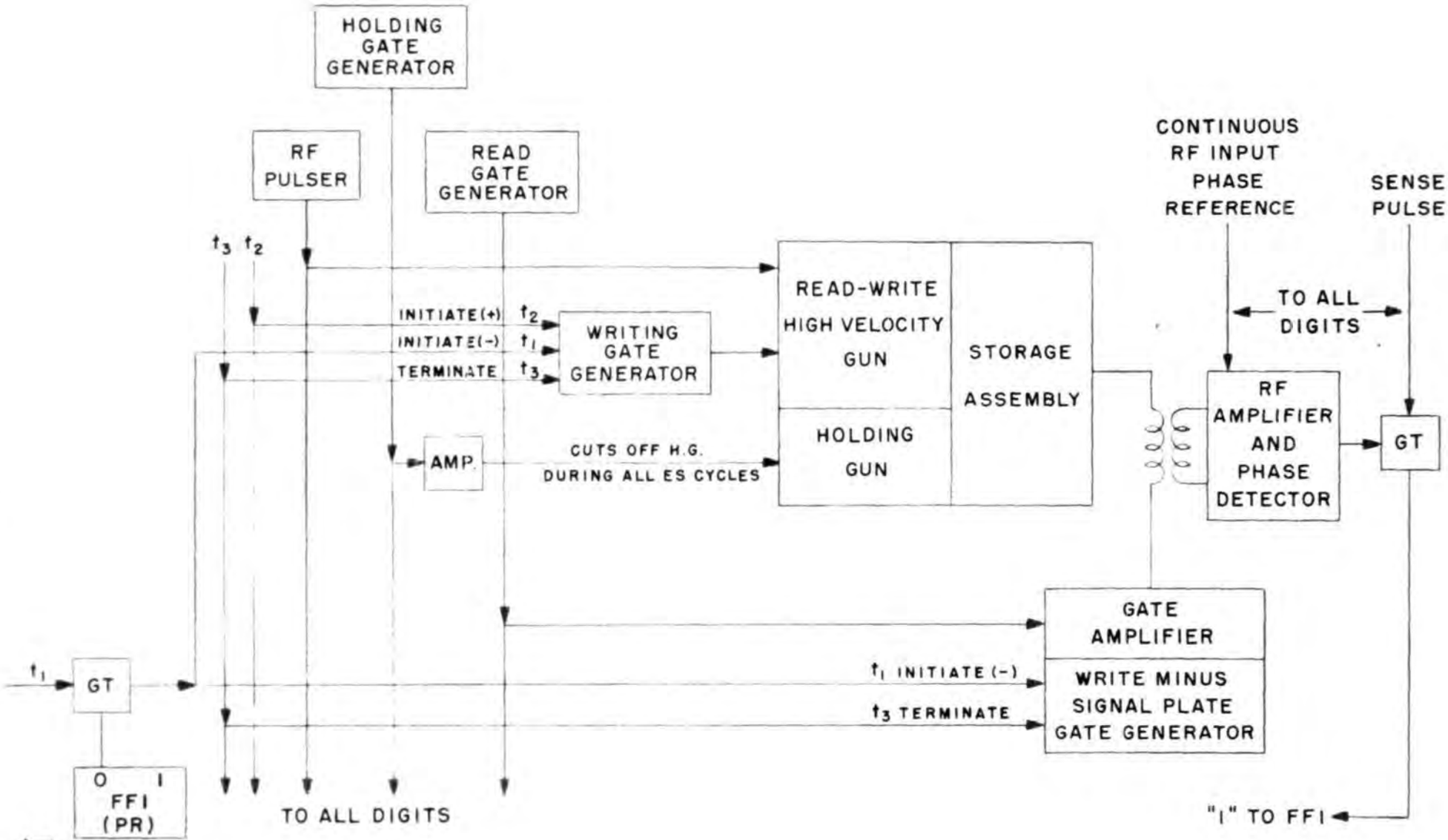


FIG. 9

SCHEMATIC

ELECTROSTATIC STORAGE DIGIT COLUMN : INITIAL SYSTEM

immediately via the flip-flop. It is one of a register of 16 called the "Program Register".

All the writing-gate generators are reproduced in each digit column, and have controls so that the requirements of the individual tubes can be met. The timing of all gates and of the sensing pulses is determined centrally in ES control. The writing gates are initiated by the separate pulses, t_1 and t_2, because the net current to the surface is different for write-plus and write-minus with the same value of beam current.

2.2 Control Circuits

The control consists of a combination of pulse counters* and pulse distributors.* Four flip-flop counters are used so that a total of 16 micro-seconds delay between any two time pulses can be realized with a 1 megacycle pulse input frequency. By presetting the counters, any time delay between successive pulses up to 16 μ seconds is available in steps of 1 μ second. The output of the counters is a series of pulses serially distributed in time as desired. The pulse distributors then separate the pulses and send each to its appropriate circuit to perform its functions. In addition to its operations on the storage tube circuits, each pulse sets the counters so that the next pulse will emerge after the desired delay, and sets the pulse distributor so that the next pulse will come out the proper operation line. The two pulses which control the initiation of the write operation go through a separate control circuit which provides a duration which is different for rewriting after a read cycle than for the write cycle. The last pulse of each cycle is returned to central control to stop the supply of 1 megacycle pulses and restart the computer in its operations.

The write cycle (see figure 7) in this system requires four control

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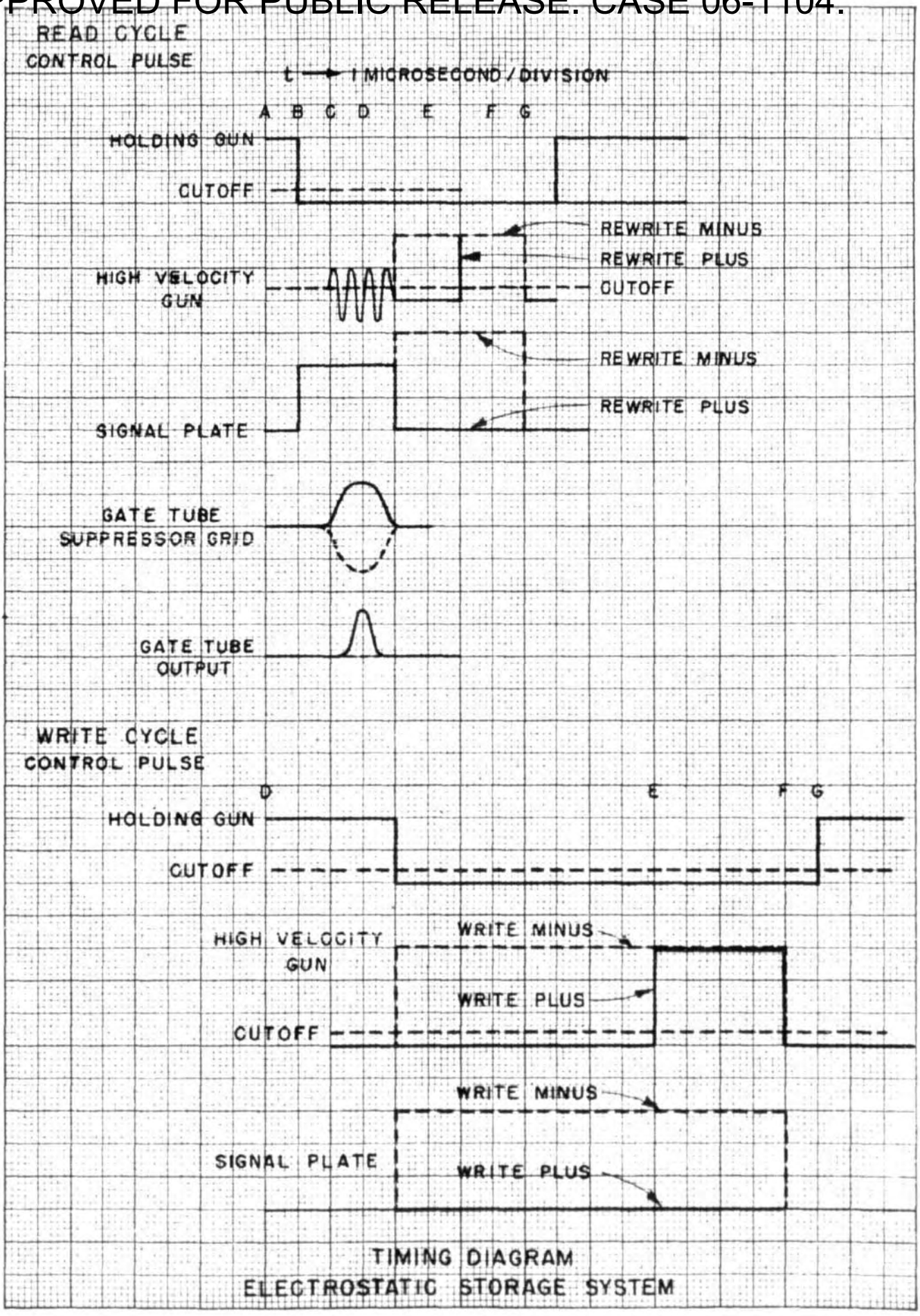
* Glossary: A.5



TIMING DIAGRAM
ELECTROSTATIC STORAGE SYSTEM

FIG. 7

A-36458

pulses from ES Control. They include pulses D through G, and their functions are shown below:

D Turns off holding guns.
Senses Program Register and initiates W-gates in those digits containing "0".

E Initiates W+ gates.

F Terminates all writing gates.

G Turns on holding gun (and restarts computer).

The writing gate amplitudes on each storage tube are the same for write-plus as for write-minus. Since the net surface current is different for the two operations, the duration of the gates must be different (figure 8). When writing a negative spot positive, the net current at the spot is $(\delta - 1)$ I, where I is the primary beam current. When writing a positive spot negative, the surface current is I. For an I common to both operations, the write-minus time must be ideally at least $(\delta - 1)$ times the write-plus time.

The read cycle uses 7 time pulses, as shown in figure 7. The last 4 pulses are functionally identical with the corresponding pulses of the write cycle. For the sake of reliability, the sensing pulse is generated from the same control pulse that initiates the RF pulser, and is delayed in time about 1.6 microseconds to allow the RF pulse to reach its full amplitude at the output of the amplifier.

2.3 Decoders and Deflection Circuits[6]

The decoders and deflection circuits position the beams in all storage tubes to the desired storage register. The present capacity of 256 storage registers requires 8 ($2^8 = 256$) "address" digits to be used. The address is used in two sections. Each of the two groups of four digits is fed to a flip-flop decoder, one of which provides the vertical deflection, and one

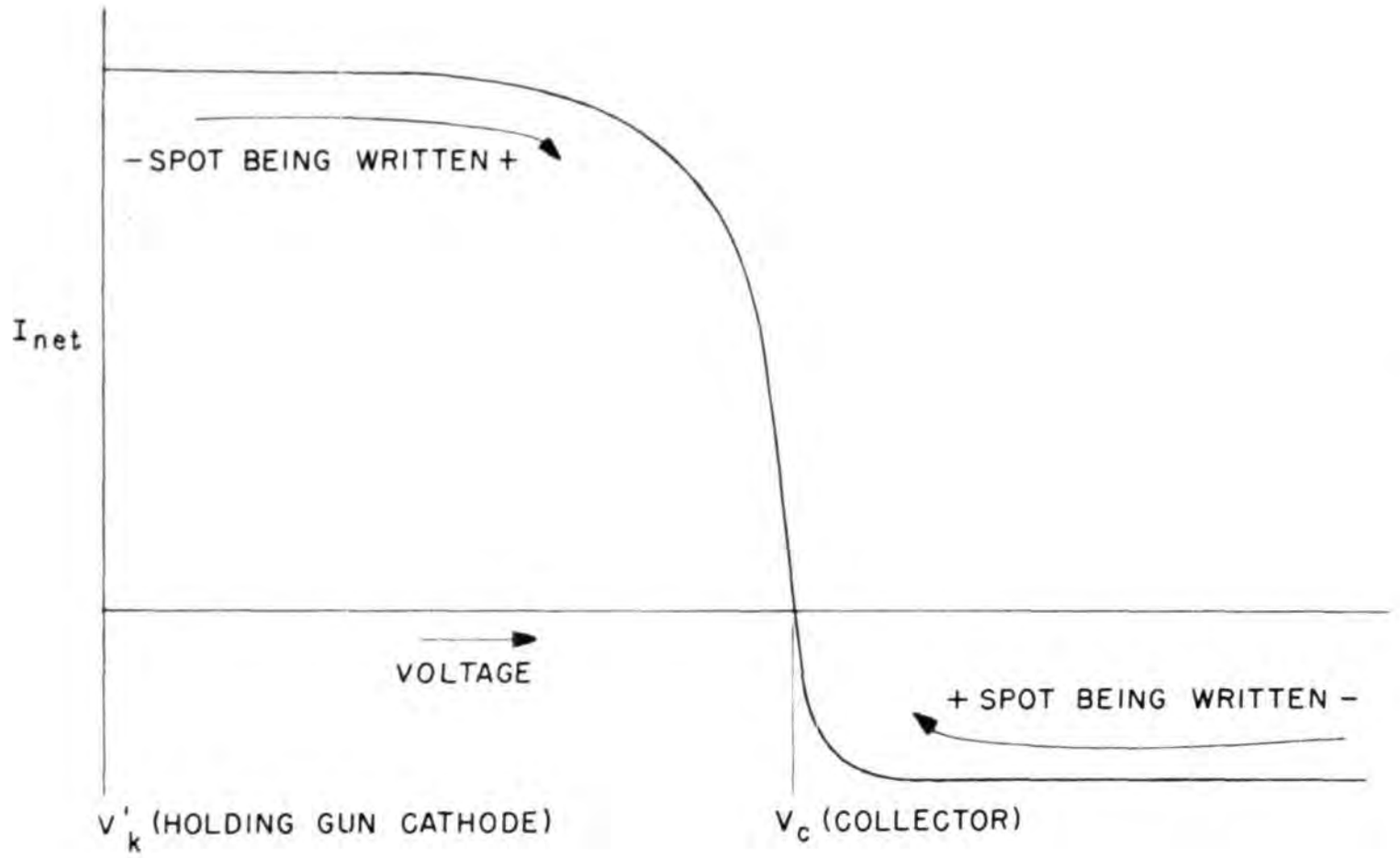


FIG. 8

WRITING CURRENT vs. SPOT POTENTIAL

the horizontal deflection. The decoders are set up a few microseconds prior to the ES operation. Each digit simultaneously switches a current source into a load resistor; the voltage across the load resistor is the input voltage to the amplifier. The current sources in each decoder are binary-weighted so that 16 levels of output voltage, corresponding to the 16 vertical and horizontal positions of the array, are available. The deflection amplifiers are stabilized by feedback and compensated to give a rise time of about 1 microsecond. The entire system is balanced; that is, each side of each flip-flop switches a separate current source. Each side of each decoder has a common load resistor and the deflection voltage for each axis is taken from the plate leads of two deflection amplifiers via a low impedance transmission line.

CHAPTER III

TEST PROCEDURES

3.1 Voltage-Variation System

Testing of the storage system, even from the early stages of installation, cannot be adequately discussed without describing the most important tool available. This is the ability to vary the voltage on any important circuit in the ES system, such as on an electrode of the storage tube. Control of the voltage-variation system is centralized so that its use is easily applicable to the entire system.

This facility, provided in the computer from the start, was intended to serve two important purposes. First, it was intended as an aid in measuring the margin of safety in timing and pulse levels at the time of installation of the circuits, and as such an aid in evaluating the design of individual elements. Second, it was intended to provide for efficiently maintaining the entire system in a high degree of reliability. In principle, the voltages on significant electrodes of the flip-flops, gate tubes, and amplifiers in the system could be varied in such a manner as to inhibit their operation. The failure point was measured in terms of the variation applied, and the condition of the circuit was evaluated as a function of the allowable deviation.

By making this facility available in the ES system, it was possible to check the operation of the circuits and of the important parameters, both gate amplitudes applied to the storage tubes and the electrodes on the storage tube itself. The limits on the various conditions were then used to find the optimum settings. In effect, the relationship of writing gate amplitude to the holding gun voltages, or spot size, or spot growth, in a particular tube or on the row as a whole, could be determined readily. Voltage-variation was used from the first to locate existing circuit troubles, prevent actual failures

by predicting them, evaluate circuit design, determine the best operating conditions for the storage tubes, and, to a limited extent, measure the effects of aging after the system was set up.

3.2 Simulation of the Computer Central-Control by Test Equipment

During the initial testing of the system, the central-control elements of the computer were not available. It was consequently necessary to replace the central control by a simulator. The simulator was composed of test equipment, mostly standard units developed for use in Whirlwind computer development. The test control was of necessity a compromise between the flexibility provided by Whirlwind and the flexibility which could be provided by the test equipment with its limited functions. The limitations imposed by this compromise have important bearing on the significance of the results of the initial tests.

The variety of conditions of operation in Whirlwind with ES can be bracketed by two extremes: (1) the condition of sensing or writing the contents of a register after some long period of inactivity, with assurance that the information was correctly read or written in the proper position on the surface, and (2) the condition of reading or writing, or a combination of the two, at random registers or positions on the surfaces at high speeds. The fact that ES is the principal memory element of the computer indicates that ES will continually be called upon to operate at least once per basic machine order, and most often twice per order. However, these conditions depend on the availability of the large capacity memory to store the program, i.e. the addresses of the numbers which are to be operated on, the numbers themselves, and the operations involved. This facility being unavailable, the problem is to approach it to some extent with the equipment available.

The first extreme of conditions, that of low frequency operations, was met by providing means for reading and writing at "pushbutton" rates,

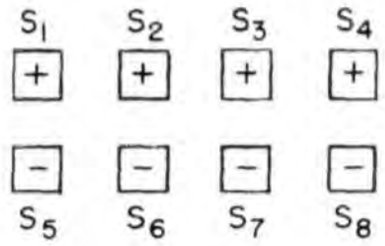
rates controlled entirely by manual intervention. The second condition, particularly with respect to random operations being carried on at random locations, could not be closely approximated with the available equipment. The test control was equipped to provide, in terms of operations, continuous reads, continuous writes, or alternate reads and writes. The deflection was set upon consecutive spots by connecting the deflection decoders as counters, and the proximity of the spots could be varied by changing the current source in the decoders. In order to determine the effects of the repetition rate on operation, the control was provided with the facility for starting and stopping operations, either multiple or single, at pushbutton rates, and at frequencies up to about 100 cps by a low frequency blocking oscillator. Furthermore, the interval between single operations could be varied from about 10 microseconds to about 2500 microseconds by inserting a multivibrator delay unit in the restart line.

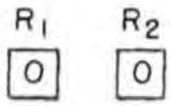
3.21 Cycling Tests

The most extreme dynamic operation which the test control provided was the so-called "cycling" test. The cycling test used the reading and writing facilities of the storage tubes to impress one of a variety of test patterns on the storage tubes, and at some time later to read out the pattern and shift it to consecutive registers. The original information was in this way retained, although its location on the storage surface was continually changing.

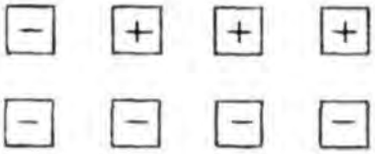
As a simplified example, consider two 4-spot rows of an array in which the top row has positive spots (1's) and the second row negative spots. Two auxiliary flip-flops, R1 and R2, are provided and are initially cleared to "0" (figure 14A). The content of register R2 should be considered to be that of the last spot, S8. The cycling operation proceeds as follows:

The content of S1 is read to R1, after which the content of R2 is

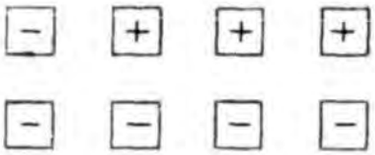




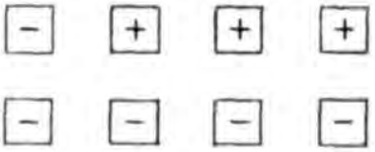
A. INITIAL CONDITION OF ARRAY



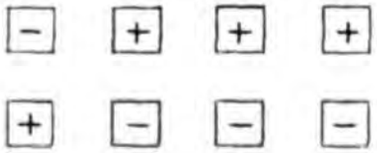
B. ARRAY AFTER ONE READ-WRITE OPERATION



C. ARRAY AFTER SECOND READ-WRITE OPERATION



D. ARRAY AFTER THIRD READ-WRITE OPERATION



E. ARRAY AFTER EIGHTH READ-WRITE OPERATION (FIRST FRAME)

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CYCLING OPERATIONS

FIG. 14

written on S1. The storage pattern is then as shown in figure 14B. R2 now contains useless information.

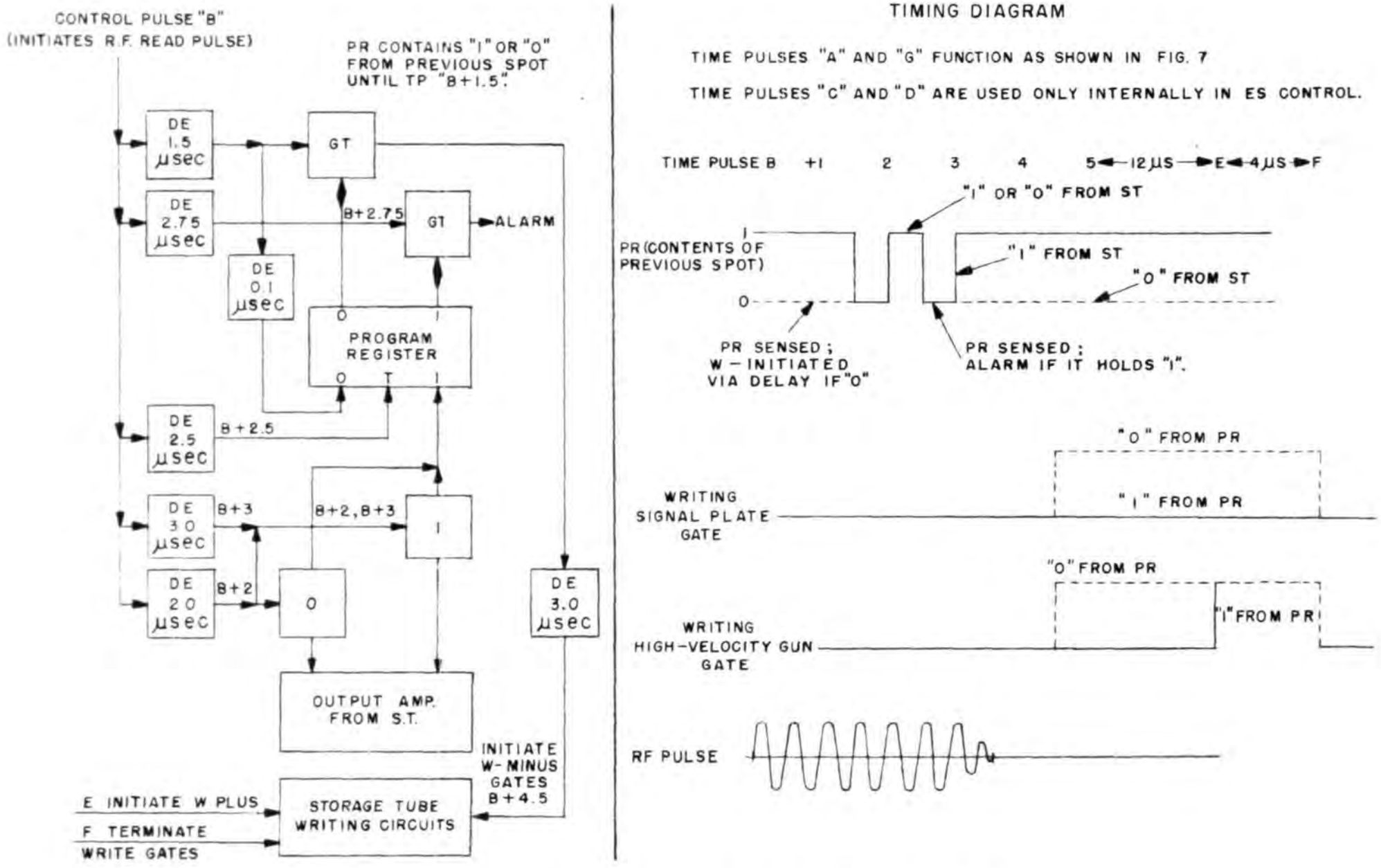
Next, the content of R1 is shifted to R2, and the beam is deflected to operate on S2. S2 is read to R1, and R2 is written on S2, as before. The data is now stored as shown in figure 14C.

The content of R1 is again shifted to R2, and the beam is deflected to S3; the above procedure is repeated, leaving the data as shown in figure 14D.

When the beam is finally returned to S1, the entire pattern is shifted one position in the array (or frame), as shown in figure 14E. The original data is intact; the pattern can be easily checked during the process by displaying the content of each spot as it is read to R1, at a position on a display scope corresponding to the position of the spot in the array. Positive readouts are made to intensify the display scope whose deflection plates are connected to the deflection transmission line. In this manner, assuming that multiple errors do not compensate for each other, the operation of the storage tubes can be checked by observation at any time without interrupting the test.

In the description of the cycling tests, two flip-flop registers are shown for temporary storage in each digit column. In the test system, one of these was replaced by a 3-microsecond electromagnetic delay line, since only one flip-flop was available in each digit column. Figure 9 shows the organization and timing of the elements used with each storage digit column in the cycling tests.

This system tests first for the presence of an actual readout from the storage tube, without discriminating between zeros and ones, after which only the information to be cycled to the following spot is read out. At the initiation of the operations on a particular spot, the PR contains information



DIGIT COLUMN AS USED IN CYCLING TESTS

FIG. 9

from the previous spot, which is to be written. The PR is sensed 1.5 microseconds after the initiation of the RF reading pulse, and for any register containing a zero, the write operation becomes write-minus by switching the signal plate and initiating the writing gate. The write operation does not start until 3 microseconds after the gate tube is sensed, at which time the reading pulse is off. During this interval, the storage tube output gate tubes are sensed. The gate tube labelled "0" allows a pulse to pass if the spot being read is negative; the "1" GT allows a pulse to pass when the spot is positive.

At time pulse B plus 2 microseconds both GT's are sensed and their outputs mixed, so that if any readout occurs, a pulse will travel to the "1" side of the program register. One-half microsecond later the register is "complemented" or "triggered", putting the register in the opposite position from what it previously held. If any readout occurred, the register must end up in the "0" position. A pulse 1/4 microsecond later senses whether any registers contain "1's", indicating the lack of a readout. If a register contains a "1", an alarm pulse emerges, and stops further cycles. The indicator lights on the PR flip-flops locate the source of the alarms. If no alarm occurs, at TP B + 5 a pulse senses the "1" storage gate tubes; if a "1" is present, indicating a positive spot, the pulse sets the corresponding flip-flop to a "1".

The read and write operations are combined into a single ES cycle. At the end of the cycle, the read-write beam is positioned on the next spot and the cycle is repeated.

3.22 Limitations of the Cycling Test

Since the cycling test is the dynamic test intended to simulate to some extent the conditions required by the computer, it is important to

realize to what extent the test is sufficient. Some limitations were apparent from the beginning. These limitations are due to the fact that the order in which the spots are operated on is fixed by the method used to set the deflection. Recall that in the final system each flip-flop in the deflection decoders will receive data simultaneously. It is possible, then, that the various spots in the array can be operated on at random. Where a routine is repeated often, a few consecutively numbered spots may be read at very short intervals while other spots may be used only at long intervals. While some registers which contain orders may never be changed, others are used as storage for partial solutions and are constantly changing. In the test system, consecutively numbered spots, located adjacent to each other are always operated on in order. Consequently, no register used in the dynamic test goes unused for more than one frame.

This fact tends to obscure deterioration which might be present and long-time drift in the deflection. Each time the read-write beam is positioned, the area under the beam is either replenished or reversed in polarity; every spot has an effectively new charge condition established each time a frame is completed. The longer intervals between operations provided by the test control could be useful in locating the more obvious troubles due to deterioration and long-time drift but the only effective way of locating the subtle troubles of this nature is to use the tubes in the final system. It is principally due to faults of this nature that the initial tests provided only a first approximation to the final conditions.

3.23 Elements of Test Control

In Figure 10, a block schematic of test control is shown. It is made up of two parts, the cycling control and the pattern generator.

The cycling control is used to provide the 1 m.c. pulses to the ES control, to set the interval between successive cycles, and to provide

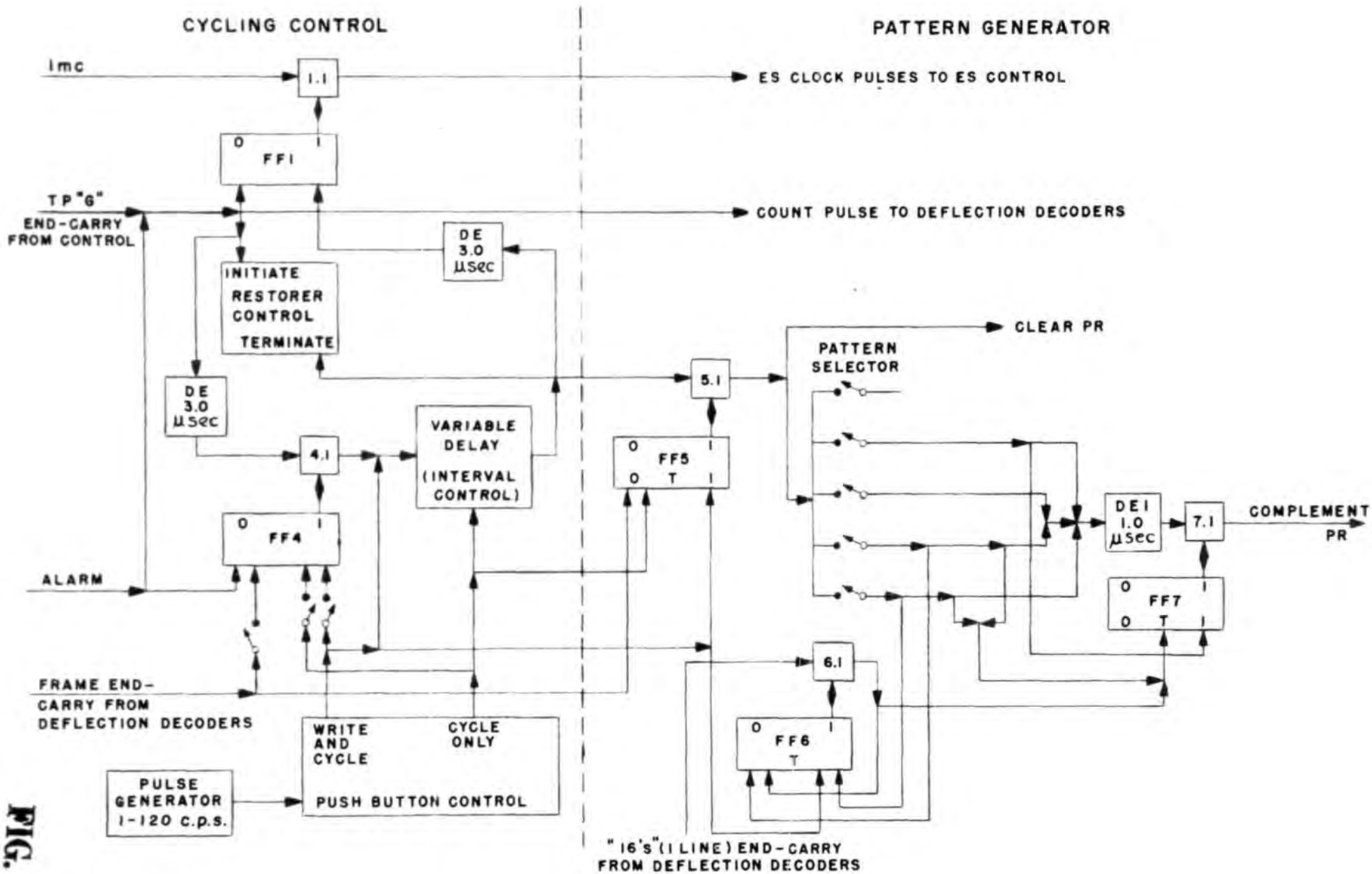


FIG. 10

SCHEMATIC – TEST CONTROL

restorer pulses* to maintain the clamping levels at the outputs of the flip-flops. The restorers are peculiar to the Whirlwind circuits and their control need not be discussed in detail as an elementary function of the test control. Restorers are furnished whenever ES is not operating, and are synchronized with the restart pulses in their control element.

The end carry pulse (time pulse "C") from ES Control, sends a "count" pulse to the deflection system, positioning the beam on the next spot. Then, after producing restorers, it senses GT 4.1. If another cycle is desired, the gate tube will be open, and a pulse will pass into the delay unit. This unit provides an interval variable between 0 and about 2.5 milliseconds between cycles. The delayed output pulse stops restorers and initiates another cycle, after appropriate delays.

The cycling operations can be stopped by an alarm pulse, by a pulse from the deflection system indicating the end of a frame, if selected, or by stopping the pulses going into the delay unit at any time.

The element which generates the patterns consists of FF's 5, 6, and 7, and their associated circuits. The pattern is determined by presetting the program register to the desired position at the beginning of each cycle. Instead of writing into a spot the contents of the previous spot, the information set into the program register by the generating system is written.

At the beginning of each generate cycle, the PR is cleared. If nothing further is done to it, a "0" will be written. If it is complemented, a "1" will be written. The various arrays are formed by combinations of clearing and complementing on successive spots in the array. A pulse from the deflection system, indicating the end of a line, is used to increase flexibility. A selector switch is used to select the desired array.

At the end of the write cycle, indicated by a pulse from the last

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* Glossary: A.4

position of the array, GT 5.1 is turned off by clearing FF 5. Data is no longer preset into the PR, so the cycling operation will automatically follow.

The write or cycle operations can be accomplished one at a time at pushbutton rates, or frame by frame at pushbutton rates, or continuously with variable interval by means of the variable delay unit.

CHAPTER IV

CHECKING THE ES CIRCUITS

4.1 ES Control

Assuming that a reliably operating storage is available and that the control is initially operating properly, a cycled pattern can be visually checked while the voltage variations are applied to the various control flip-flops, gate tubes, and driver lines. This provides a quick, rough check on overall operation of the control. In this method of testing, it is presumed that a failure of the control will change a parameter, such as HVG duration or the time of the ST sensing pulse, sufficiently to produce a failure. Any such failure would obviously be quite drastic since, for instance, a change in writing time of many microseconds is necessary, if the proper write time is 12 or 16 microseconds, before it affects the information to be stored.

This method proved to be generally ineffective, and indeed often detrimental when applied to the gate tubes in ES Control. The principal indications derived from checking GT's are due to lowering screen voltages such that the output pulse amplitudes are reduced. ES Control is essentially an open loop of counters and pulse distributors which, once initiated, provide timing pulses, the last of which terminates the cycle and returns control to the computer. If then, the counter output pulses or preset pulses are diminished in amplitude, the final result is to extend the overall time of the ES cycle. In many cases the limit is not first obvious as a change in the information in the storage tube but results in loss of restorers and consequent loss of information in most of the computer. The end result is that it destroys the indications of the failure, making the trouble location impossible. Although an indication of relative reliability is obtained, the relationship of the first failures which are intermittent to the indications of the failure may be so indefinite as to be unreliable.

Since the purpose of the control is to provide pulses which are properly spaced in time, the most fundamental method of checking its operation is to check the timing of the output pulses. A check of each timing pulse would require a duplication of the control equipment. A simpler, more economical method is to check the total time included in the ES cycle. This is not a rigorous test, since it allows the timing pulses to shift, relative to each other within the cycle as long as the final pulse emerges at the proper time. The fact that the most common type of GT failure experienced in the computer is due to a decrease of cathode emission allows the checking system to be further simplified. Since a decrease in emission due to interface in the cathode, aging, or circuit failures, produces a decrease in output signal, for the range of input pulses used the net result is to extend the overall time of the cycle. Consequently, it is sufficient to sense only if the cycle is too long. The total ES time can then be reproduced in a reasonably sensitive delay element in such a manner that the end-carry from the checking delay will cause an alarm to stop the operations only if it precedes the final time pulse. (Figure 11)

The matter is related to considerations of the possibilities of flip-flops failing. With respect to the counters, the problem is straightforward. The tendency of a flip-flop to stick in the 0 position is the same in its results as the failure of a gate tube to pass a pulse properly since sticking in the off side causes the associated gate tube to remain off. Conversely the tendency of a flip-flop to stick in the "1" position, or to stall as when the clamp circuits fail, is the same in its results as the conditions of the gate tube in passing pulses continually. Flip-flop failures in the counters, therefore, can cause an ES cycle to be shortened or lengthened. This latter possibility was checked well by the scheme shown above. The former possibility was not checked by an analogous system, since routine flip-

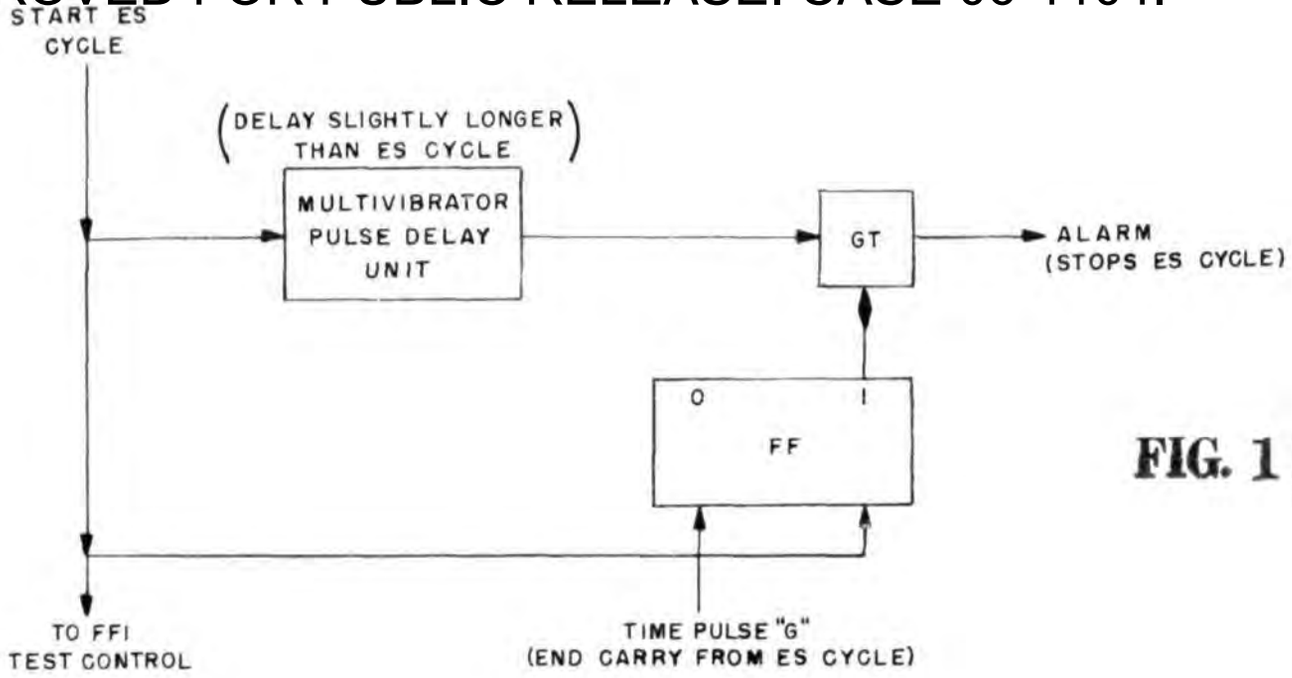
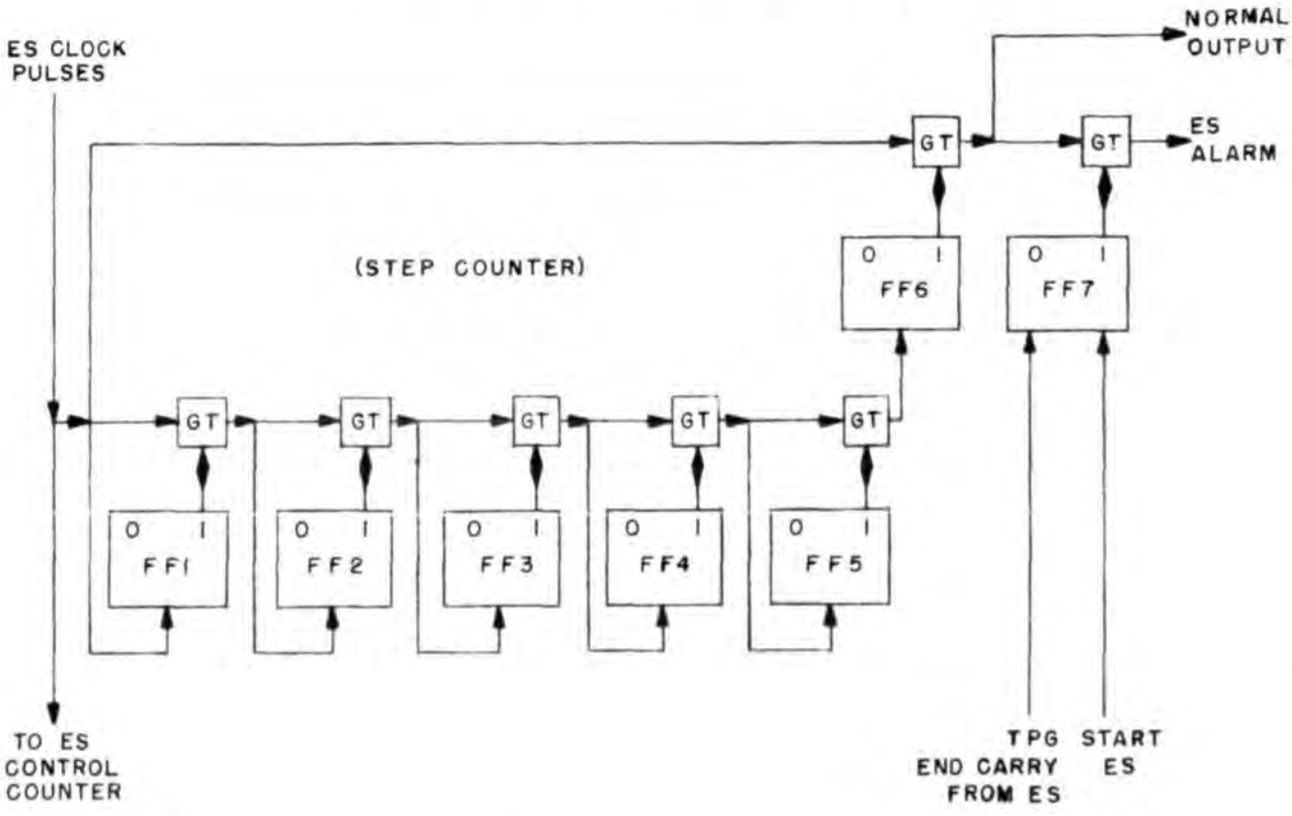


FIG. 11

TEST SET-UP
TIMING CHECK OF ES CONTROL



FINALTIMING CHECK
ES CONTROL

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FIG. 12

flop tests could be expected to maintain them in good condition. Consideration must be given to methods of checking the control more thoroughly. Although it is not unreasonable to require manual checking of certain parts of the computer, when any element is required to operate for long periods without failure an automatic checking feature becomes very desirable. In the initial testing of the storage element, so much attention was given to the manual maintenance problem that manual checking was a small burden. When the ES system assures its final role, it will be required to operate reliably for long periods of time. Its value as a part of a complex electronic system precludes the use of manual intervention for routine checking if the checking could be performed automatically.

The instability of the delay unit in the timing check system made it unsuitable as a part of the complete system. A 5-stage flip-flop counter in the computer's central control has been used in later tests to take the place of the variable delay unit. Although it actually checks only that each ES cycle is less than 33 microseconds, it was effective enough in increasing the reliability of the circuits so that it was unnecessary to increase the complexity of the system by making the timing identical. The ES timing check system is shown in figure 12. All flip flops are initially in the "0" position. The clock pulses which go to ES control counters also feed the 5-stage counter shown. Thirty-two ($32 = 2^5$) pulses are required to set FF6 to a 1; if another time pulse is present it will emerge from GT6 and provide an alarm stopping the operation. Since the last time pulse from ES control stops the flow of clock pulses, no alarm can be present if the total ES time is less than 33 microseconds. If the future conditions of the storage element, such as a significant decrease in access time, requires that the timing be checked more thoroughly it can be accomplished by modifications and additions to the counting units shown. For precise indication of a too-long ES

cycle, the counters must be preset to "0's" or "1's" in such a manner that their total counting time will equal the ES interval. By the addition of another counting circuit the system can be made to detect ES cycles which are too short. FF 7 has been added to prevent any end-carries which occur in the normal operation of the counter (the Step Counter) from giving indications of an ES failure. ES Alarm pulses can only be present when an end-carry is produced during an ES cycle.

CHAPTER V

STORAGE TUBE TESTS

5.1 Test Methods

Testing of the storage tubes and their driving circuits commenced with the conditions from the preliminary tests. The tolerances, as well as recommended values for the writing gates, the focus voltage, and the holding gun voltages, were available. After using a few of the different patterns available, it became obvious that the storage tubes were sensitive to the pattern used as well as to the other parameters. The problem then resolved itself into determining the most rigorous tests both by observing their operation in cycling and by analyzing the conditions necessary for their operation.

The best results as indicated by observing various cycling tests were obtained by the use of two complementary patterns. The first required a single negative spot to cycle through an array of 255 positive spots. The second required a single positive spot to cycle through an array of 255 negative spots. By varying the writing gates by means of the voltage-variation circuits during the cycling operation, the limits of the useable gate amplitudes were measured. Detection of errors was made more accurate by observing the output signal on an "A-scan" of each frame. The sweep was initiated by a pulse at the start of a cycling frame. Decreasing amplitudes of the output signals were also investigated as a function of their position on the surface and any spots in the array which were difficult to switch due to shorted mosaic squares or imperfections in the mica were immediately apparent.

The investigations during cycling were concentrated on two parameters -- the writing signal-plate gates and the high-velocity gun gates. The other parameters, read gates, writing gun bias, and focus, were merely set to reasonable values, since their effects on overall reliability were better known. The

read gates were set equal to about 2/3 of the writing signal-plate gates. Recall that the read gate serves principally to displace the potential of a positive spot so that a signal can be produced from it as it is charging back toward collector potential. The lower limit on the read gate is then a few volts, for short pulses of reading current. The upper limit is determined by the ability of the reading beam to produce a positive signal at the signal plate. The read gate must, then, switch a negative spot to a potential less than the collector potential. In the worst case of an unstabilized negative spot, the read gate must be less than about 3/4 of V_{HO}. The range of read gates for a V_{HO} of 100 volts is then from about 10 volts to 75 volts. These values are increased slightly to provide for the voltage division due to the signal-plate to storage-surface capacity.

The high-velocity gun bias used was determined by measuring the cutoff of the gun and operating below cutoff by a reasonable margin, e.g. 5-10 volts. For convenience, the bias was adjusted within the 10 volt range to provide for the most uniform signals on the static TV display.

The focus voltage was chosen more or less arbitrarily for the best contrast at the edge of a plus spot on the static display. The settings were justified by observing the effects of varying the focus while cycling an arbitrary pattern. The effects were not significant over a range of 50-100 volts.

5.2 Limits on the Writing-Gate Amplitudes

Before discussing the significance of the optimum settings of the writing gates, it is well to review the writing operation in greater detail.

The effectiveness of a writing operation is measured with regard for the stable potentials under holding gun action. In order that a spot be considered positive, its potential must be in the range above first crossover;

similarly a spot to be considered negative must lie in the potential range below first crossover. In either case, with sufficient time under the action of the holding gun, a stable potential will be reached, i.e., a point at which the current to the spot is zero. It is true and pertinent that it is difficult dynamically to determine the potential of a particular spot; the polarity of the read-out signal is dependent on the potential of the spot under the read-beam and on the amplitude of the read gate applied. Any spot at a potential in the negative stability region can be made to read-out a positive signal by applying a read gate whose amplitude is greater than the voltage between the spot and the collector, since the high-velocity beam always charges the spot toward the collector voltage. Any spot in the positive stability range can be made to furnish a negative signal by using a read gate whose amplitude is less than the difference between the spot potential and the collector voltage. The theoretical optimum value of read-gate amplitude, in order to best distinguish between positive and negative spots anywhere within their respective stability ranges, is equal to the collector-to-first-crossover voltage difference.

The problem of distinguishing between positive and negative spots in their unstable regions is complicated by the variations which exist over the surface in the capacity from signal-plate to storage-surface to collector. The capacities form a voltage divider network. The fraction of a read gate, for instance, which actually is applied to the storage surface at a particular point depends on the thickness of the mica and the collector-to-surface spacing at that point. Variations of 15% are not unusual. If the distinction between spots in the two stability regions were dependent only on the read gate, the variations in the capacities as well as noise variations originating in the gate generating and amplifying circuits would make the distinction impossible.

For this reason, the write operation is required to supply sufficient charge to write the spot to a potential as close to collector voltage as possible, and, when writing negative, switch the spot to a potential as close to the negative stable point as possible. Under such conditions, the read gate amplitude is not critical.

Due to the secondary emission phenomena, the requirements for write-plus and write-minus are quite different. The cases of writing a plus spot positive and writing a minus spot negative can be considered trivial in this respect, because the charge transferred to the respective spots is negligible. When writing a negative spot positive, the total current to the spot is equal to

$$I^{-} = (\delta - 1) I_b$$

where I_b is the primary (high-velocity gun) current. When writing a positive spot negative, the net current is I_b, because the secondaries are attracted back to the surface. For a given beam current, writing minus requires $(\delta - 1)$ times the writing time that a write-plus operation requires. The original design of the writing circuits provided for the same gate amplitude for writing plus and writing minus. The durations of the gates were different and were variable in the 1 microsecond's steps provided by the control counters. The variables to be determined were the gate amplitudes each of which could be set for the particular storage tube and the gate lengths, which were necessarily common to all the tubes.

The data in table I contains the limits on the amplitudes of the gates in eight digit columns. The data is typical of conditions in the row in the cycling tests, and was taken without specific reference to the theoretical requirements in the various tubes. The write minus gates, for instance,

TABLE I

MARGINS ON GATE AMPLITUDES IN ES COLUMNS

	Polarity of Single Spot (255 Spots are Opposite)	Write-Minus Signal-Plate Gate (Volts)		High-Velocity Gun Gate		Read Gate		$V_{HG}=V_C-V_K'$
		Lower	Upper	Lower	Upper	Lower	Upper	Fixed
1	Positive	83	106	<50	91	37	104	90
	Negative	81	145	<50	>130	25	94	
2	Positive	93	130	46	113	< 25	105	100
	Negative	78	> 200	53	95	< 25	105	
3	Positive	80	123	49	105	48	100	96
	Negative	78	200	40	>120	25	105	
4	Positive	85	128	<45	98	< 25	98	90
	Negative	82	160	<45	112	<25	107	
5	Positive	95	135	<45	125	25	110	108
	Negative	93	>200	45	>125	25	107	
6	Positive	115	157	40	>125	< 25	144	100
	Negative	115	>180	< 50	>125	< 25	130	
7	Positive	95	125	60	76	< 25	110	100
	Negative	103	160	60	112	< 25	92	
8	Positive	90	129	43	90	<25	100	98
	Negative	82	132	48	109	<25	107	

were not set directly to the theoretically optimum value determined by V_{PG} and the voltage division due to the signal-plate-to-surface capacitance. Similarly, the high-velocity gun gates were not set to produce a specific value of beam current. The measurements were solely system-wise, determined by cycling the two test programs. The data points out some of the weaknesses of the cycling test for lining up the storage tubes.

In each digit column, the maximum allowable signal-plate gate is greater when cycling a single negative spot than when cycling a single positive spot. If the testing conditions were ideal, the values should agree closely. In each case the higher value of signal plate gate caused an ensuing positive spot to disappear; a single write-plus following the write minus was insufficient to switch the negative spot. The lower maximum value is nearer what would be expected due to the voltage division in the capacitances. Since the values used were purposely chosen without careful consideration of the theoretical optimum, the most reliable conditions were considered to be those from which maximum deviation could be safely tolerated; in other words, the operating conditions should be the values midway between the two limits. Table I shows the differences in these limits for two patterns. The limits, and consequently, the optimum settings, varied between the values in table I for different patterns. The values chosen were, in fact, closer to the center value of the limits taken with a single plus spot cycling on a negative background. Two factors influenced the setting. The first of these was consideration of the reliability of the chosen conditions for different patterns, such as a single positive line. The limits for the latter were nearer the values for a single positive spot. The second factor was a consideration of an approximate theoretical limit. Knowing the value of V_{PG}, and

using an approximate value of voltage division (6/6), the W-gate required to write a spot just to the negative stability point was determined. For a closer approximation the value would be subject to correction of the capacity-division ratio and the variations in the ratio over the surface of the tube. As an operating value, it would be further corrected for expected variations in gate amplitude due to noise and repetition frequency. In spite of including these two factors in setting the gates, reliable operation over periods longer than a few hours was not achieved. Moreover, many tubes showed a reluctance to start cycling at high speeds, although once cycling they seemed to operate well. In short, the dynamic tests used did not provide the conditions for suitably reliable operation. It is possible that reliability could have been achieved by using a greater variety of patterns; the task of analysing the results derived from a number of patterns would almost undoubtedly reduce to theoretical considerations, which could be carried on independently of cycling.

5.3 Results of Cycling Tests

The cycling tests provided three important indications of weaknesses in the system. The first was that interaction between neighboring spots was not tolerable, even in cycling tests; the interaction caused positive spots occasionally to be switched below first-crossover voltage when the high-velocity gun was used on adjacent spots. This phenomenon had been observed before and investigated more fully that was possible in the ES Test System; it is due to the secondary electrons emitted by the high-velocity beam being attracted to adjacent positive spots which are at a voltage higher than the collector by the amplitude of the signal-plate gate. The deterioration of the spot depends on the current in the writing beam and on the polarity of other adjacent spots, as well as on the capacity between spots and to the signal-plate.

The effects of interaction for a given center-to-center spacing between spots can be diminished by limiting the use of the high-velocity gun and by drawing as many of the secondaries away from the surface as possible. The first of these factors was accomplished by the "selective-write" operation, which writes a spot only when its polarity needs to be changed. The writing system was modified so that before each write operation, the spot to be written is sensed. If it corresponds to the polarity to be written, the writing gates are not initiated. The method of accomplishing this is discussed in more detail in the description of the final system. A further attempt to limit the use of the high-velocity gun by eliminating rewrite was unsuccessful. The rewrite is particularly necessary when a negative spot is read. The rate of charging to the collector potential under high-velocity gun action is greater than the charging rate of a positive spot, and the positive spot can deteriorate about 4 times as much without switching.

By using a reading pulse of less than two microseconds, and a low reading current, the positive spot will be charged only a few volts, and at the termination of the read operation will restore more rapidly to collector voltage under holding gun action.(Figure 5). It was proposed that, by using a read gate of the same amplitude as the writing signal-plate gate, the potential of a negative spot would not be affected by reading, and would always return to the negative stability region following the read operation. By adjusting the write signal-plate gate so that at the end of a write- or a read minus operation the spot would be returned to the point of maximum negative holding-gun restoring current, the most reliable setting should be obtained. This method was rendered ineffective by the extreme variations of the signal-plate gate which exist over the surface of some tubes and by stray feed-through signals to the amplifier. The method depends on a null read-out

from a negative spot. If, for any reason, the read gate is larger than the write-minus gate, a slight positive output signal will result from reading a spot shortly after it is written negative. The extremely low negative charging rate indicates that 2 volt variations cannot be tolerated within 100 microseconds of write or read operations. The signal-plate gate variations, due to capacity-division, would cause some areas to be written below cathode potential; the area would eventually charge in a positive direction to the cathode; the ensuing read-out would then be positive.

The second important weakness was the inability to erase a positive spot by a write-minus operation. The beam current in writing plus and minus is identical, since the gate amplitudes applied to the high-velocity gun are identical. Although the total charge to a spot was controlled by using different writing times, this did not assure that a positive spot would be completely erased in writing times up to 16 microseconds. A reliable method of completely erasing a positive spot of reasonable size was to provide a larger beam diameter for writing negative; this was accomplished by increasing the high-velocity gun drive for writing minus over that for writing plus.[8] The final schematic of the system shows the manner in which the two gates were controlled.

The third principal source of failures was due to deflection shifts which occurred during cycling tests. The deflection generators and amplifiers were eliminated as a source of the failures by installing a cathode-ray tube with a phosphorescent surface which used the same type of gun and deflection plates as used in the storage tube. The tube was subjected to the same drives (writing, reading gates and deflection voltages) as used on the storage tube, and various spot positions were observed and measured for shift using a

machinists microscope. Since no shifts were observed, the trouble must have originated within the drift space of the storage tubes; it was observed in various degrees, on several tubes. The fault was assured to be due to glass-charging on the bare portions of the tubes, and has recently been measured in the laboratory on a tube which had exhibited severe deflection shifts in the system. An attempt to eliminate the glass-charging has been made in a modified design of the storage tube which includes no bare portions of glass between the guns and the storage surface.

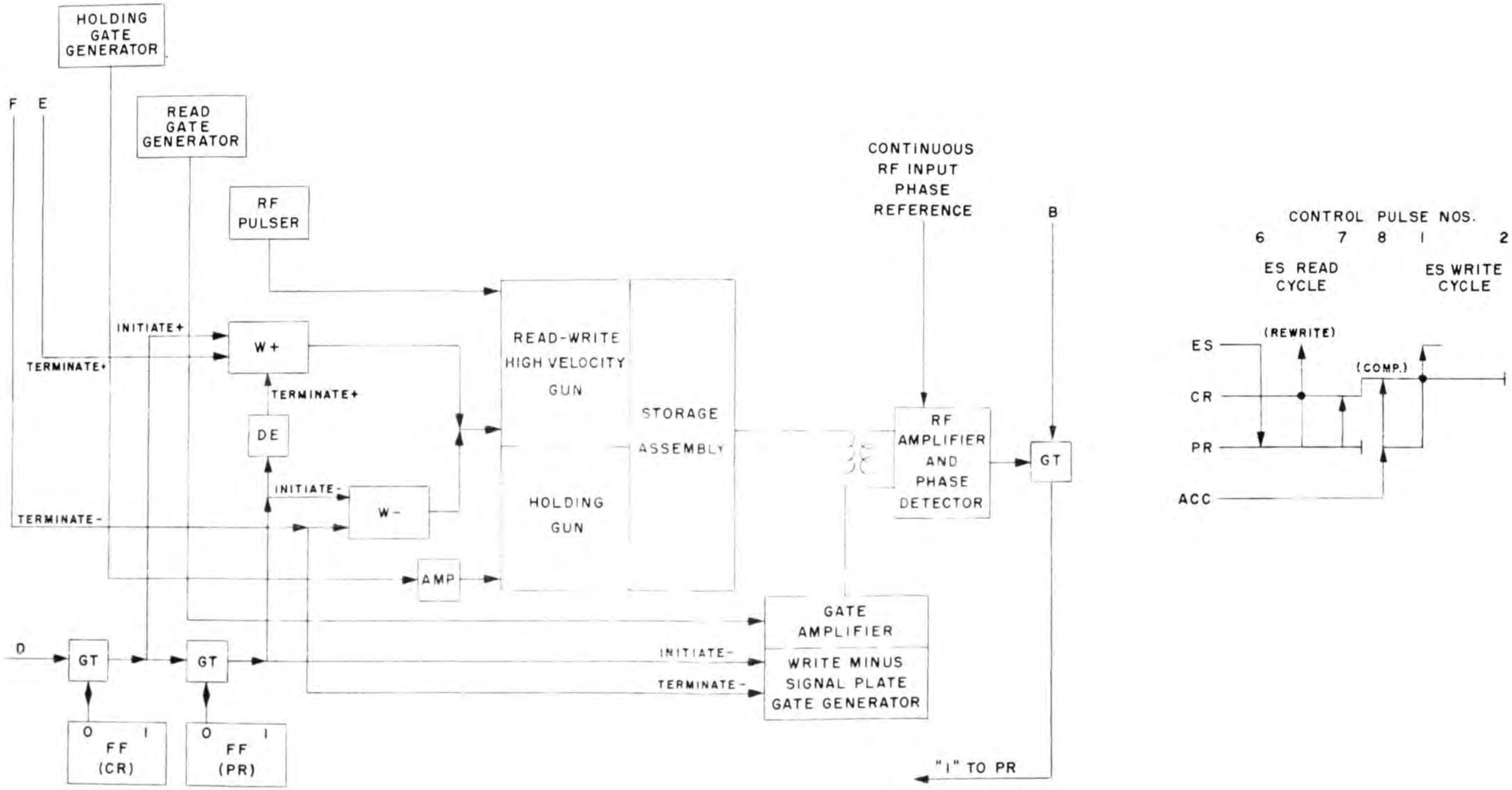
CHAPTER VI

FINAL PHASE OF TESTS

6.1 Selective-Write System with Separate Writing Gates

The design of the ES system as it was incorporated into the Whirlwind system for the final phase of the initial tests was affected by the results of the cycling tests and of other dynamic tests conducted in the Storage Tube Reliability Tester. The system includes means for reading from a storage register prior to each write operation and comparing the data to be written with the contents of the register; a write operation is performed only in the locations where the data is to be changed. To overcome the difficulty of erasing, separate writing-gate generators (high-velocity gun) were provided, the write-minus gate having the higher value. The block schematic of the system is shown in figure 13. In the timing diagram, the numbered pulses refer to Whirlwind central control pulses, the lettered pulses to ES control pulses. Any operation which requires writing (TP "1") must include a previous read (TP "6"). An extra flip-flop register (Check Register) is used as a means of comparing the old data with the new data, and allows the write operation to be performed in those columns where the data is to be changed. The ES timing cycle for the read and write operations is similar to that of the old system. The comparison for selective-write takes place at the command of the computer control.

The read operation is the same as before, with the exception that the rewrite takes place via the CR. The CR is cleared at the start of a read cycle so that the information in all digits of the register will be rewritten. The pulse ("D") which initiates the rewrite senses the CR. Since it holds a "0" in all digits, the output of the CR in each digit initiates the write-plus gate, and also senses the PR in the same digit. If the PR holds a "0", the write-minus gates will be initiated, and the write-plus gate will be



BLOCK SCHEMATIC
ES COLUMN AND SELECTIVE WRITE CIRCUITS

FIG. 13

terminated through a short delay which prevents the gate generator from being pulsed while it is switching "on". Pulses "E" and "F" are used to terminate the writing gates separately, providing separate control for the write-plus and write-minus intervals.

At the end of a read cycle, the content of the storage register is in the PR. If the read is associated with a write operation, the data to be written is present in a computer arithmetic register, the Accumulator (AC). The "old" data is read to the CR from the PR is cleared. The new data is then read both to the CR and PR, after which the CR contains "0's" in all digits where the new and the old data differ. In order to clarify the system, an example will follow, using a 4-digit word.

Data to be Written: 1001 (AC)

A read operation is performed on TP "6", after which the PR contains, for example: 1010.

PR 1010

CR 0000

The PR is then read to the CR and cleared,

PR 0000

CR 1010

after which the CR is complemented.

PR 0000

CR 0101

The AC is read simultaneously to the PR and CR. In all digits where the datum to the CR is a "1", the CR will be complemented.

PR 1001

CR 1100

The following write operation (TP "1") will be effective only in the last two digits.

6.2 Final Operating Conditions

Preliminary to the useful operation of the storage system with the computer, the entire system was available for the final phase of the initial tests. With the flexibility of the computer's control circuits providing an almost indefinite variety of procedures, each controllable parameter was then reset using tests specifically designed to provide an optimum setting. Most careful consideration was given to the RF system and to the writing gates. For purposes of completeness, a brief description of the method used to set the gain of the RF system follows.

6.21 The RF System

Initially, attempts were made to use a standard gain setting for the output RF amplifiers, using the noise at the detected output as a measure of the gain. Differences in the transfer characteristics (bias voltage vs. beam current) of the high-velocity guns, the presence of RF feedthrough signals of varying amounts and phase, and possible variations in the input impedance and signal-to-noise ratio of the amplifiers made this ineffective. In order to reach a reliable line-up routine, it was necessary to include all these factors. This was accomplished by setting the high-velocity gun bias safely below cutoff, and adjusting the amplifier gain to the threshold value for which the output signal caused the gate tube to conduct. A substantial safety factor was achieved by using a 5:1 attenuator at the input to the amplifier.

6.22 Writing Gates

The bases for setting the high-velocity gun gates were principally two:

1) Spot size,

2) Transfer characteristics of the storage tubes.

The spot size was measured by observing positive arrays on the TV display. Since separate write-plus and write-minus gates were available, a positive spot of any size could be switched by using a write-minus gate of slightly larger amplitude. The limits on spot size were determined by the expected deflection shifts, by the interaction effects of writing minus on adjacent spots, and by the center-to-center spacing of the spots. Because of the presence of the severe deflection shifts due to glass-charging, the interaction was more or less disregarded; it was compensated for by inserting holding-gun time after each cycle to restabilize the affected areas. In effect, large spots were tolerated at the expense of MS operation time. The spot size was increased until it was about equal to the center-to-center spacing. A further increase would make the write-minus critical, since it would damage the adjacent spots.

The spot size is determined, to a first approximation, by the product I x t, where I is the beam current and t is the duration of the writing pulse. Since the two are nearly interchangeable, it was possible to compensate for an increase in one by a decrease in the other. A study of the transfer characteristics of the tubes, taken at the time of the production tests and again at the time of the latest tests, indicated that in the ranges of decreasing bias the decrease in current was increasingly serious. It was necessary, for purposes of reliability, to operate with as low currents as possible, using long writing times. The control circuits limited the writing times to 32 microseconds, and the desirable spot size was achieved by beam currents of about 20 microamperes. For most of the tubes, this value of current lay in a reasonably stable region of their characteristics.

The write-minus high-velocity gun gates were set so that nearly complete erasure was obtained with 16 microseconds writing time, and complete

erasure at 32 microseconds. The corresponding beam currents were within a few microamperes of, generally higher than, the write-plus currents.

The signal-plate gates were set with regard for three factors:

1) The potential in the negative restoring region where maximum charging rate occurs,
2) Noise in the gate generating circuits,
3) Deterioration and long time drift in the gate amplitudes.

The first factor is important because in order that a spot be written reliably negative, it should be switched at least into the region of maximum restoring current. The variations in the capacity division from signal-plate to surface to collector required a compromise in the attempts to write nearer to holding-gun cathode voltage. In tubes with severe variations in the capacity division, the gates were set to write to the region mentioned, although it meant that some areas might be written below holding-gun cathode. Also, in order to minimize spot interaction, it is important to minimize the switching voltage. This factor was not significant because of the extra holding-gun time used to nullify the major source of interaction, the spot size. The region of maximum negative restoring current is shown in figure 5 to be about 10 volts below 1st crossover. First-crossover was measured by writing negative over the surface with decreasing gate amplitudes, and observing the amplitude for which spots first failed to write-minus. Noise, due to the sensitivity of the circuits to repetition rate and to power line transients, and deterioration due to long time drifts in the gate-amplifier circuits, were expected to require about 10 volts increase in the optimum gate as a safety factor. The final value of the gate was set at 20 volts above the value measured as the minimum gate. The read gates were set nearly equal to the 1st crossover to collector voltage, to obtain the best discrimination between negative and positive areas.

6.3 Conclusions

6.31 Circuit Reliability

Although the cycling tests did not produce reliable storage tube operation, they did indicate a few weaknesses in circuit design, particularly noise sources in the gate amplifier circuits. A more significant result was the development of techniques for testing the circuits on a routine basis. The control section was checked by the built-in method discussed in chapter 4. The driver circuits were tested functionally, that is, as they affected the information which was transferred to or read from the storage tube. Even with the relatively unreliable conditions of the storage tubes during the cycling tests, it was possible to maintain the circuits in a high degree of reliability. When the final phase of testing began, the circuits were eliminated as important sources of trouble. The testing procedures have not been changed significantly in the newer RS system.

6.32 Storage Tube Reliability

After setting up the system according to the methods of section 6.2, the entire computer was able to operate for as long as 8 to 10 hour intervals, and has been used steadily for shorter periods. This has not only provided opportunity for studying the more complex problems which require the large storage capacity, but it has provided the facility for checking certain parts of the computer which had been hitherto unchecked because of the lack of an independent storage element. Where failures have occurred in storage, the problem of locating their sources has been more straightforward than in the cycling tests. The principal difficulties have been with properties of the storage tubes. These faults are being studied carefully, so that future design changes can include their correction.

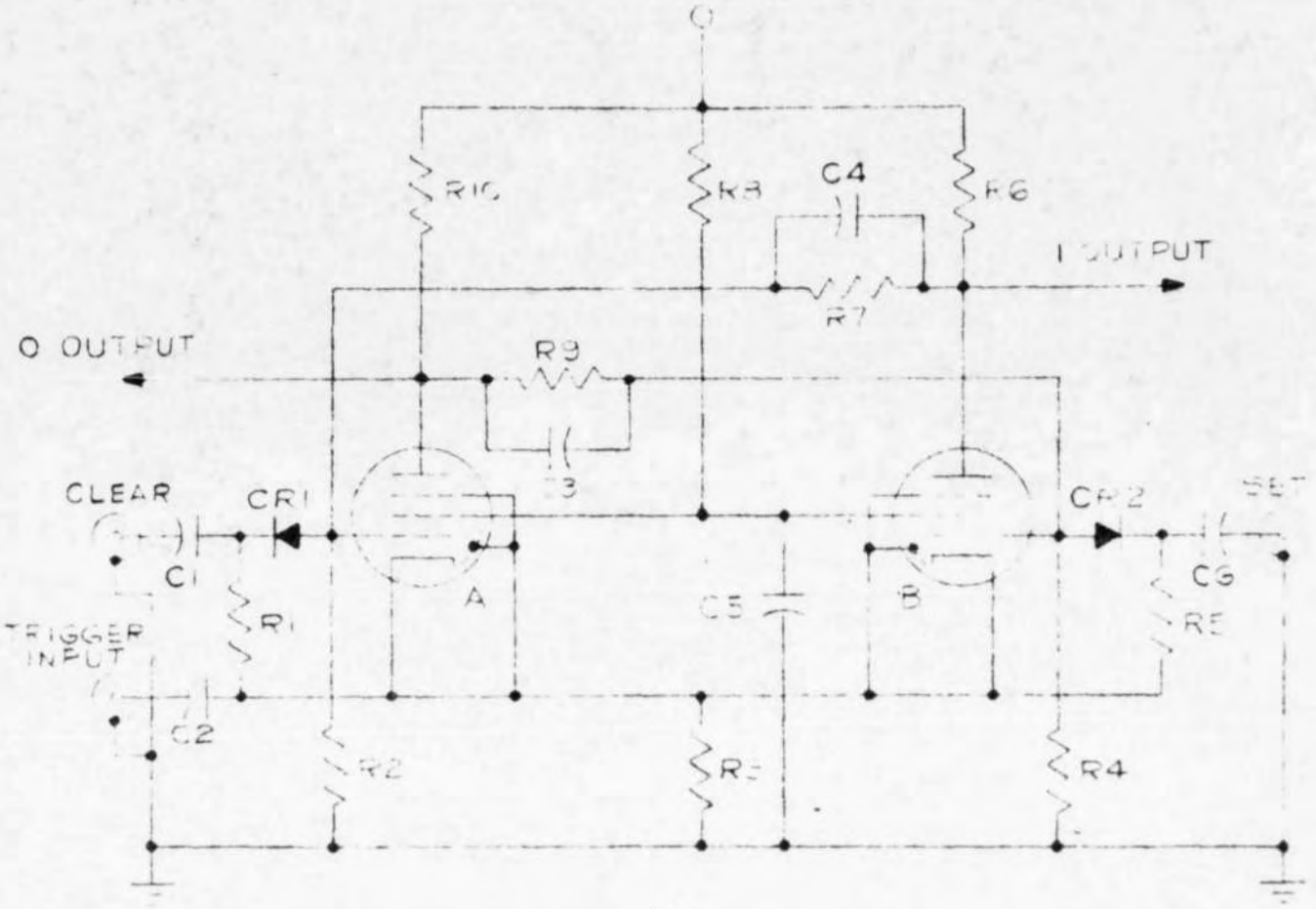
Shifts in deflection and deterioration of the writing guns must receive principal consideration. The former is the most serious, because it appears to be random and uncontrollable in the present tubes. It determines the lower limit of spot size, is a factor in the severity of interaction, and consequently, is the most significant factor in determining the effective access time. When a decrease in spot size is possible, the access time will be limited by interaction and by the writing times. Although interaction is produced most notably by writing minus, an important contribution toward eliminating it would be provided by eliminating rewrite. Although rewrite is only about 1/10 as long as writing, it occurs about 5 times as frequently. Effectively, then, rewriting accounts for about 1/3 of the interaction. The rewrite cannot be eliminated without decreasing the variations in the signal-plate-to-surface and surface-to-collector capacities, nor without a more exhaustive study of the noise problems in the RF system.

GLOSSARY

A.1 Electronic Digital Computer

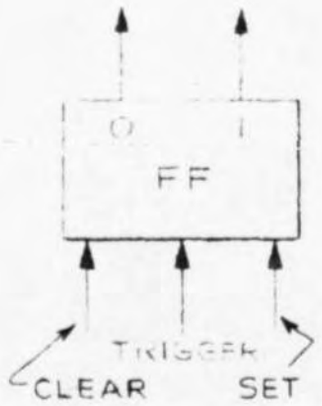
A digital computer is a machine which performs sequences of arithmetic operations on numbers which are represented as digits, rather than in terms of physical quantities as used in analog computers. Electronic, digital computers perform their operations by means of vacuum tubes and their associated circuits. Their most distinctive characteristic is their high speed in comparison to electromechanical machines. The Whirlwind Computer can perform 10,000 additions per second. For purposes of simplicity and reliability, numbers and the orders which control the operations on the numbers are represented in a binary fashion, that is, as combinations of "1's" and "0's". In Whirlwind, numbers are used in their base-2 representation. Each digit of the number is stored and operated on in elements which have only two stable states, one state corresponding to a "1", the other to a "0". Whirlwind is a 16-digit parallel machine; all digits of a number are stored and operated on simultaneously. The group of elements which contain the complete number is a 16-digit "register". The content of each element is transferred to other elements as a voltage pulse; the presence of a pulse usually corresponds to a "1", the absence of a pulse is a "0".

The most basic circuits of an electronic binary computer are the flip-flop and the gate tube. (Figures 15 and 16) The flip-flop is the bistable element in which information is stored during the basic arithmetic operations. The gate tube is a coincidence element used to sense the state of a flip-flop. One grid of the tube is tied to the plate of the "1" tube of the flip-flop so that when that flip-flop tube is conducting the gate tube is off, and vice versa. The gate tube is sensed at the desired time by a pulse applied to the control grid; a pulse will emerge from the gate tube if the other grid is "on".



(a)

FLIP-FLOP CIRCUIT DIAGRAM

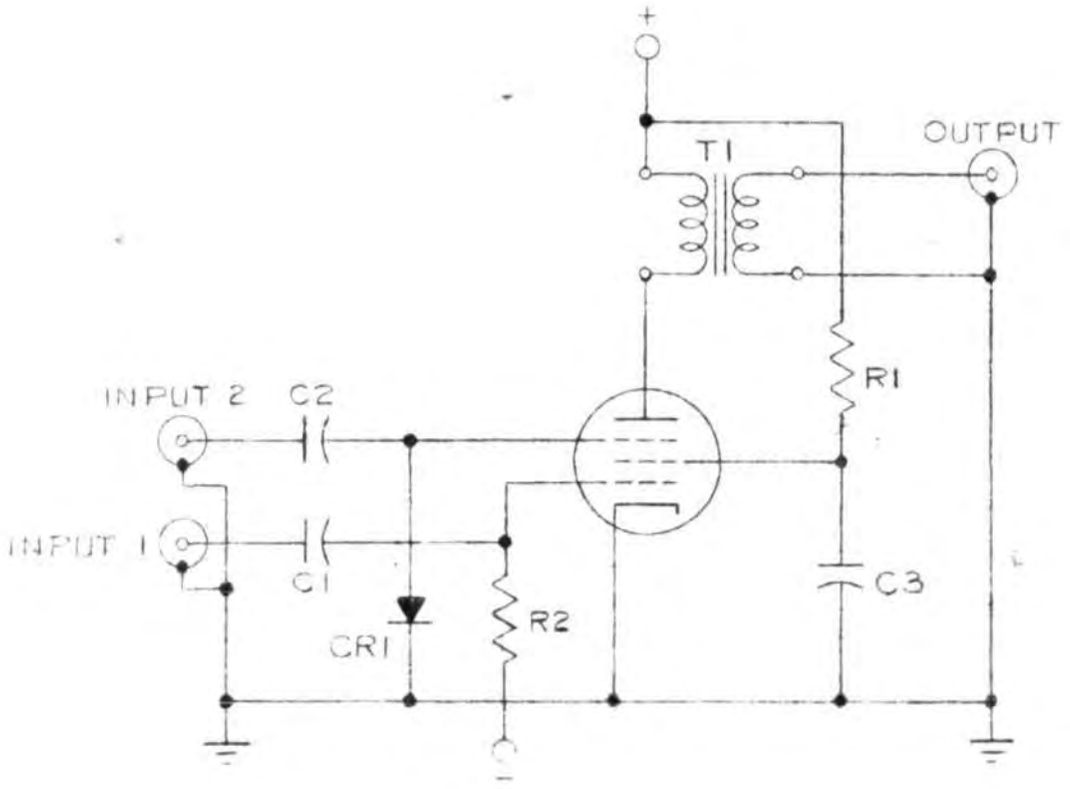


(b)

BLOCK REPRESENTATION OF FLIP-FLOP

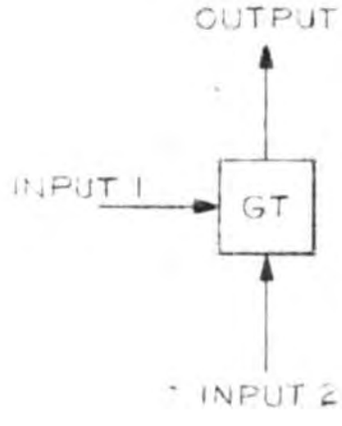
A-3519

FIG. 15



(a)

GATE CIRCUIT
(INPUT 2 FROM FLIP-FLOP)



(b)

BLOCK REPRESENTATION OF GATE CIRCUIT

A-35170

FIG. 16

A.2 Gate

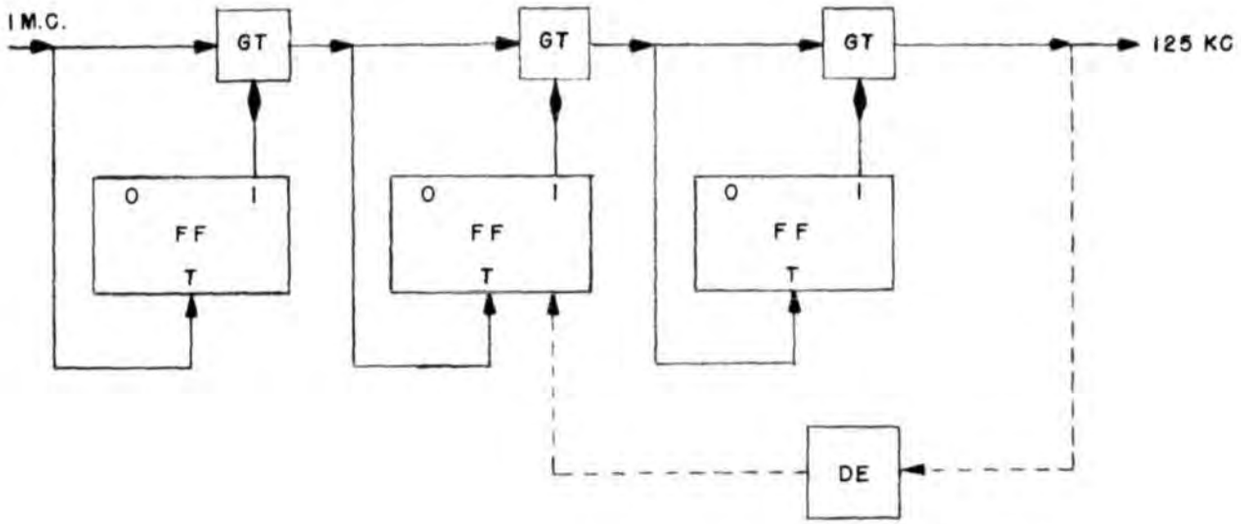
A gate is a voltage pulse whose duration is long compared to its rise and fall times; it is essentially flat-topped. Gates are generated in the storage system from flip-flops. The plate of one of the flip-flop tubes is coupled to an amplifier. The duration of the gates is determined by pulsing the grids of both flip-flop tubes, once to initiate and once to terminate the gate.

A.3.1 Flip-flop counter

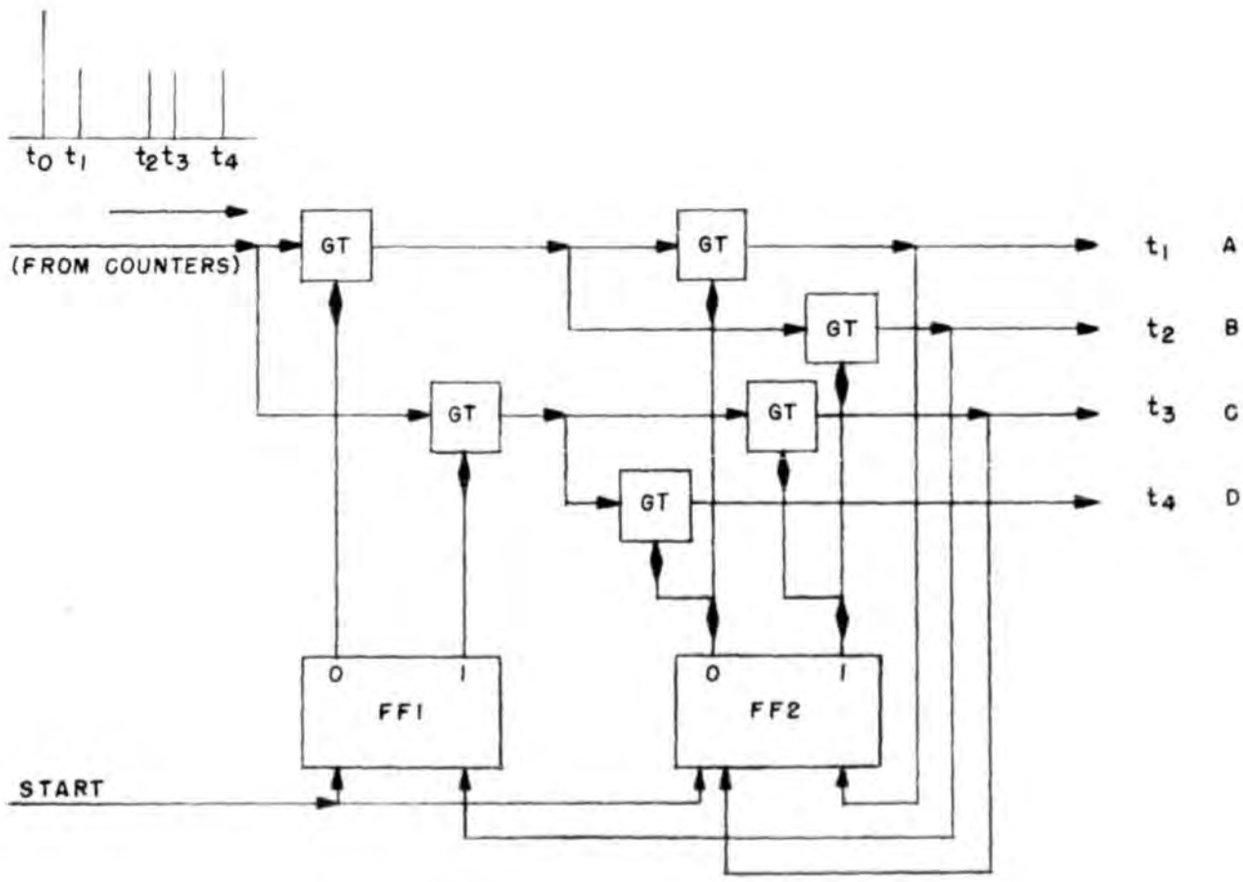
A group of flip-flops can be made to count or divide down input pulses when connected as shown in figure 17. The 3-stage counter shown will divide 1 m.c. input pulses by 8 ($= 2^3$) when connected as shown in solid lines; since each input pulse to each stage sets the flip-flop alternately to "1" and "0", every other input pulse will emerge from each stage. By using each output pulse to preset the flip-flops, as shown in dotted lines, the basic dividing factor can be decreased.

A.3.2 Pulse distributor

An array of flip-flops and gates can be made to distribute a number of successive input pulses over a number of output lines, which may control individual operations, as shown in figure 18. The input pulses are on a single line; as each pulse emerges from the appropriate gate tube, it sets one of the flip-flops so that the next pulse emerges on the next line. Each output pulse controls a certain function, so that the overall timing is fixed by the timing of the input pulses. In the storage system, each output pulse also sets up the counters to provide the desired delay before the next pulse appears at the input of the pulse distributor. Any pulse can then be delayed from 0 to 16 microseconds from the preceding pulse. In the storage system four flip-flops are used in cascade to provide 7 output pulses.



FLIP-FLOP COUNTERS FIG. 17



FLIP-FLOP PULSE DISTRIBUTOR FIG. 18

A-36465

A.4 Restorer Pulses

Restorer pulses are used to maintain the charge on the coupling capacitor from a flip-flop plate to the gate tube grid. A pair of pulses are applied to the flip-flop cathode periodically, generating a square wave at the plate which restores the charge on the capacitor which was lost due to leakage through the back resistance of the clamping crystal.

Signed..Richard.W..Read....

Approved.....
Jay W. Forrester

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