Code: 03.069.460
Date: April 2, 1953

ENGINEERING EXPERIENCE IN THE DESIGN AND OPERATION OF A LARGE SCALE ELECTROSTATIC MEMORY

by

J. C. LOGUE, A. E. BRENNEMANN & A. C. KOELSCH

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March 24, 1953

ABSTRACT

The development and operation of a high speed, large capacity electrostatic memory for use with large scale scientific computers and data processing machines are described. The video amplifier and deflection circuits are considered in detail.

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INTRODUCTION

The electrostatic memory discussed in this paper was built to provide a moderately large storage capacity with relatively high speed access. The primary objective was to design a satisfactory electrostatic memory, for large scale scientific computers and data processing machines.

This paper will include discussions for the engineering considerations encountered in the design and operation of the circuits involved. The video amplifier will be described and the factors involved in setting the amplitude discriminating level of the video amplifier will be treated in detail. The deflection circuits will be discussed, together with the special requirements of electrostatic storage and how these requirements were met.

It should be mentioned that the design of this computer was made to conform to the concept that the programmer must not be restricted because of spill. This concept together with what seemed to be an attainable spot density, namely 512 bits per cathode ray tube, required that the machine operate with a maximum read-around ratio of 171 to 1. In the process of achieving this read-around ratio, a new effect was discovered which caused loss of information. This effect, named "mudhole," will be described with methods for minimizing it.

Whenever necessary a description of circuit operation will be given to assist the reader in understanding the problems and their solution. A brief general description of the machine is included.

GENERAL DESCRIPTION

This electrostatic memory was developed specifically for the IBM Type 701 Electronic Data Processing Machine. It is a parallel machine, using a stored program, which performs arithmetic operations using binary representation. Machine specifications dictated that electrostatic memory provide facilities to store 3048 full-words. It was felt that this memory capacity could be achieved with two memory frames and that it might be achieved with one memory frame. A full-word consists of 36 bits including a sign bit. A full-word is used to represent a number only, while a half-word of 18 bits may be used to represent either a number or an instruction. When a half-word is used as an instruction, one bit represents a sign, five bits are used

to select one of the 32 possible instructions and 12 bits represent the address upon which the instruction is performed.

Figure 1 shows the electrostatic memory with its 36 memory drawers. Each memory drawer contains two 3 inch cathode ray tubes. The deflection system and its power supplies are located in the enclosure on the right side of the frame. In the interest of accessibility and ease of maintenance, this section of the memory frame is hinged.

MEMORY TIMING CYCLE

A major objective in the design of the electrostatic memory was to reduce to a minimum the time required for regeneration. The original cycle was to be of 10 microseconds duration. However, it was found that by increasing this cycle 20%, two addresses could be regenerated during one cycle. Thus the fundamental cycle was established at 12 microseconds and the time required for regeneration was thereby reduced to nearly one-half.

The "regeneration" cycle permits two addresses to be regenerated, while the "use" cycle, also of 12 microseconds duration, permits one address to be interrogated. A "use" cycle implies that the arithmetic unit either reads information from memory or writes information into memory. If the arithmetic unit is performing an operation which does not require a reference to memory, memory is automatically regenerated.

A cycle timing diagram is shown in Figure 2. A "use" cycle is shown at the top of the figure. The relative timing is indicated by the vertical dashed lines spaced 2 microseconds apart. This "use" cycle applies to either the left or right cathode ray tubes. Left and right refer to the physical location of the cathode ray tubes in the drawers. It is seen that the sample pulse is almost coincident with the dot unblank pulse. The dash unblank pulse and the dash generator pulse which is applied to the horizontal deflection plates, are seen to be nearly coincident.

At the bottom of Figure 2 is shown the "regeneration" cycle. In this cycle the left cathode ray tubes are unblanked first and the information obtained is recorded by means of a trigger circuit in each memory drawer. The right cathode ray tubes are unblanked 2.5 microseconds later and another trigger circuit in each drawer records the information obtained. These two trigger circuits condition two "and" circuits, so that a dash may be replaced in the cathode ray tubes if needed. In this way, two addresses, one in each group of 36 tubes, are regenerated during one "regeneration" cycle. On the average there are three "regeneration" cycles per arithmetic operation.

MEMORY DRAWER

One of the engineering objectives in the design of the memory frame and

its associated equipment was to obtain unitized construction thus achieving accessibility and interchangeability. Figure 3 is a picture of a memory drawer. The high-voltage circuits and the intensity and focus potentiometers are located at the back of the drawer. The video amplifier and switching circuits are located on the right side of the drawer.

The function of the circuits in the drawer is to translate the state of charge existing on the tube phosphor to signals which can be interpreted by the arithmetic unit. Conversely, they permit signals from the arithmetic unit to be converted to the proper state of charge on the screen of the tube.

SWITCHING CIRCUITS

Figure 4 shows in simplified block form the circuits associated with the left cathode ray rube. To illustrate how the circuits operate, let us consider a "use" cycle during which the left cathode ray tube is interrogated. If a dash signal is obtained at the output of the video amplifier, the sample pulse will be suppressed by the type 1680 inhibitor tube, thus preventing the trigger circuit from operating. This in turn will condition the "and" circuit so that the dash unblank pulse will be permitted to unblank the grid of the cathode ray tube. While the beam is on for 3 microseconds it is moved horizontally about 25 mils. The dash is thereby replaced and the memory bus has remained at its lower level of -30 volts, indicating to the calculator that a dash is stored at this address in this particular drawer.

When a dot signal is obtained at the output of the video amplifier, the sample pulse will not be suppressed by the type 1680 inhibitor tube and the trigger circuit will change its state. This causes the dash unblank pulse to be suppressed by the "and" circuit thereby regenerating the dot. The memory bus is raised to its upper level of +10 volts at the time the trigger circuit is made to operate.

VIDEO AMPLIFIER

The video amplifier should have a short recovery time, good noise figure, and stability against gain variations. In addition to these requirements, it was necessary for the amplifier to fit into a reasonable space and be straightforward in design for ease of servicing.

The "regeneration" cycle makes the recovery problem rather critical. As was mentioned previously, during the "regeneration" cycle the right tube is unblanked 2.5 microseconds after the left tube. This means that the amplifier has about 1.5 microseconds in which to recover. If the amplifier were allowed to have a good low frequency response the recovery problem would be exchanged for a microphonic problem and the decoupling filters could not be made to fit into the space available. In addition to making the time constant of the coupling circuit for the 5th stage less than for the other stages,

the time constant of the input circuit of the amplifier was made very short. This solved the recovery problem but increased the noise problem.

It might be well to explain the need for making the input time constant short in order to ease the recovery problem. The input time constant is equal to the product of the stray capacitance of the pickup plates and the input resistance of the amplifier. As can be seen from Figure 5 the input resistance used is 20,000 ohms. The input circuit has a stray capacitance of 35 micromicrofarads. To understand the effect of a change in the time constant of the input circuit let us assume the time constant is large. With a large time constant for the input circuit, a dot signal will appear at the grid of the input tube as a negative pulse. A dash signal will appear as a positive going step voltage at the time the beam interrogates the screen of the cathode ray tube and a smaller positive going step voltage will be superimposed on the first at the time the beam is shut off. It can be seen that if a dash signal is obtained from the left cathode ray tube, the signal will be present when the right cathode ray tube is interrogated during the "regeneration" cycle. For this reason an input circuit with a short time constant was found to be necessary even though it caused the signal to noise ratio to be deteriorated. A very short time constant obtained by making the input resistance on the order of 1,000 ohms would almost eliminate this resistor as a source of noise. This would require an amplifier with a wider bandwidth since the signals appearing at the grid of the first stage would be very short duration pulses.

In order to have a good noise figure the input impedance of the amplifier should come near to matching the source impedance. This is not possible since the pick up plates have a low shunt conductance. The resulting noise figure is on the order of 200 or more. High noise figures are not desirable but can be tolerated if the noise has little likelihood of overriding the signal. We shall show later how frequently noise can cause a signal to be misinterpreted.

The circuit diagram for the video amplifier is shown in Figure 5. The video amplifier has five stages of amplification using type 6CB6 tubes and the sixth stage uses a type 6AS5 tube. Attenuators are used to couple the signal out of the sixth and seventh stages for observation on an oscilloscope. The half-power bandwidth of the video amplifier extends from 210 kc to 1.6 mc. Stability against gain variation is achieved by leaving the self bias resistors unbypassed.

Figure 6 shows the signals that appear at the output of the 6th stage of the video amplifier. These actual photographs, from a typical memory drawer, show all 512 signals superimposed during a series of regeneration cycles. The signals at the top of Figure 6 are dash signals from the left and right cathode ray tubes. Dot signals are shown below the dash signals. A left sample pulse is shown at the bottom of Figure 6, to demonstrate its timing with respect to the peak of the left dot and dash signals.

As long as a dash signal is larger than 9 volts, as measured at the plate of the 6th stage, the sample pulse will be suppressed. If the dash signal is less than 9 volts, it will be interpreted as a dot. This 9 volt level is called the discriminating level. Its value was arrived at by making certain assumptions. One assumption was that spill will reduce all dot signals to zero volts. This is a pessimistic assumption. Another pessimistic assumption was that the gain of the video amplifier might change by a factor of 2 in either direction. An optimistic assumption was that only thermal and shot noise would be present. In this connection, a question of critical importance is, how frequently can white noise cause signals to be misinterpreted?

$$n = \frac{\Delta f}{2\pi\sqrt{3}}\, e^{-\frac{V_0^2}{2\overline{E^2}}} \qquad (1)$$

n = number of noise pulses per second which exceed a voltage V_0.
Δf = effective bandwidth.
$\overline{E^2}$ = mean square noise voltage.

The equation above has been shown [1] to express the number of noise pulses per second which may be expected to exceed a voltage, V_0. From this equation it is seen that n is a very rapidly varying function of the discriminating level, V_0.

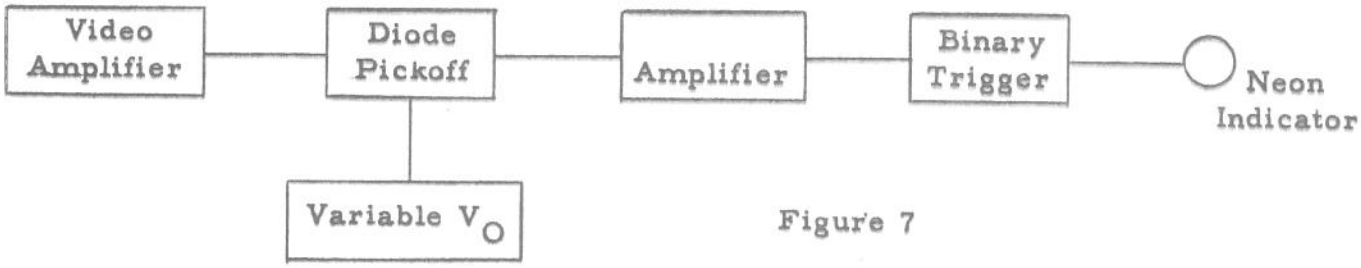


Figure 7

Equation (1) was checked by means of the circuit shown in Figure 7. The voltage discriminating level, V_0, for the diode pickoff was adjusted until one pulse per second was indicated by the neon indicator. Since this is a statistical phenomenon, this count of one pulse per second was averaged over a period of about a minute. Using a figure of 1.4 mc. for the effective bandwidth and a value of V_0 as determined above, the value of $\overline{E^2}$ was calculated by means of equation (1). $\overline{E^2}$ was also measured using standard techniques. The values of $\overline{E^2}$ as obtained by these two methods, checked very well.

[1] Lecture of "Theory and Properties of Noise Waves" given in June 1950 at the IBM Poughkeepsie Laboratory by Professor David Middleton of Harvard University.

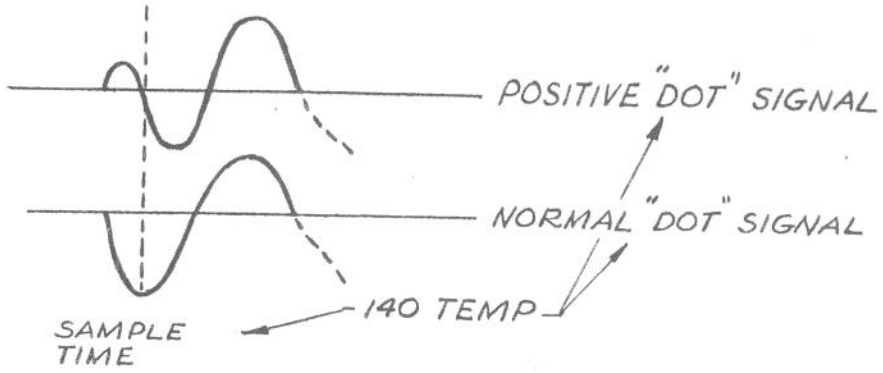
The 9 volt discriminating level, as referred to the plate of the 6th stage of the video amplifier, was determined in the following way: With the gain of a video amplifier set to a normal gain of 70,000, the binary trigger shown in Figure 7 was found to count at a rate of 60 counts per minute when the diode pick-off voltage, V_0, was set at 2.3 volts. One count per year per drawer was considered to be the maximum rate at which noise could cause signals to be misinterpreted. From equation (1) it was found that pulses larger than 4 volts should occur no more frequently than once per year. If the gain can increase by a factor of 2 then the 4 volts will become 8 volts and 9 volts is still a safe voltage discriminating level. The same reasoning was applied to a dash signal and again a value of about 9 volts was obtained. In this case it was assuming that the gain decreased by a factor of 2. Thus it is seen, that even under the worst possible operating conditions, white noise cannot cause signals to be misinterpreted more frequently than once per year per drawer.

OPERATING EXPERIENCE

When the memory drawers were placed in operation certain problems arose. One was the observed change in signal amplitude at the output of the video amplifier. If this change was severe, information was lost. Investigation proved that vibration of the pickup plates caused modulation of the signals. Molded rubber holders were developed which prevented motion of the pickup plates with respect to the cathode ray tubes. In addition they permitted easy installation and removal of the pickup plates. After installation of the rubber holders this trouble disappeared. The glass pickup plates which we employ are coated with a conductive material and allow visual inspection of the raster.

Originally, in the alignment of a drawer, the intensity was adjusted to less than intensity saturation. With this intensity setting a change in the amplitude of the unblank pulse will cause a change in the amplitude of the dash signal. It may be seen that the amplitude of the unblank pulse is determined by a clamp voltage shown in Figure 8. To compensate for a change of the clamp voltage, the resistor, R_k, shown in Figure 8 provided degeneration to minimize the amplitude variations of the dash signal.

The resistor, R_k, however, created an undesirable condition called "positive dots". A "positive dot" is compared to a normal dot signal in Figure 9.



If the initial positive excursion of this undesirable signal is of sufficient amplitude, at sample time, it would be interpreted as a dash signal. It is our belief that this condition is due to the change of the cathode potential caused by two currents flowing through R_k. One of these currents is the normal cathode current and the other is the current that flows due to charging the grid to cathode interelectrode capacitance during the beam turn on time. The change in cathode potential caused the point of beam impingement to move radially as the beam was being unblanked. This in turn produced "digging" which gave rise to the initial positive excursion of the dot signal. Removal of the resistor, R_k, eliminated the "positive dot" difficulty. The degeneration that the resistor, R_k, formerly provided was compensated for by adjusting the drawer to intensity saturation. This permitted larger dash signals with negligible increase in spill and at the same time nominal variations of ±2 volts of the clamp voltage produced no appreciable amplitude changes of the dash signal.

After eliminating the previously mentioned "positive dot" difficulty a new type of "positive dot" became a source of trouble. The "positive dot" in this case was caused by capacitive coupling existing between the grid of the cathode ray tube and the pickup plate. This coupling arose due to improper grounding of the silver coating which is applied to the outer surface of the cathode ray tube. Silver plated beryllium copper fingers were used to ground the silver coating of the tube. Two factors contributed to a poor ground. First, the abrasive action produced by the removal and insertion of tubes caused silver to be worn from both the tubes and grounding fingers. Secondly, the electrolytic action of copper and silver produced an insulating film. An improved silver coating on the tube and a silver plate followed by a rhodium plate on the grounding fingers solved this problem.

Another unusual effect was observed. When a particular address in the left tube was referred to repeatedly, a dash at the corresponding address in the right tube would be regenerated as a dot. This was due to a poor cutoff characteristic of the right tube which permitted some beam current to flow to the phosphor, although supposedly it was completely cutoft. This condition was corrected by raising the clamp voltage from +30 to +40 volts.

DEFLECTION SYSTEM

The basic considerations in the design of the deflection system were accurate positioning of the beam, stability of the circuit components and voltages, and speed of response to change of address.

A circuit was tried in which digital to analog conversion of address designation was performed at a low level and the result applied to a d-c feedback amplifier. The output of the amplifier was connected to the deflection plates. In this circuit the feedback resistor was required to be non-inductive for the amplifier to have a good transient response. This resistor had an

Ayrton-Perry type of winding. The intermittent shorting together of the overlapping wires in the resistor produced transients which were amplified, causing random errors in the operation of the electrostatic memory.

In view of the above, it was found necessary to develop a circuit that did not require non-inductive resistors of the type mentioned previously. Also, if the digital to analog conversion could take place at a high voltage level, an amplifier with its possible instability could be eliminated.

A circuit was developed in which predetermined currents are switched into a summing resistor to generate the precise deflection voltages. Cathode followers are used to couple these deflection voltages to the deflection lines. The current switching circuit has the stability characteristics of a cathode follower.

In Figure 10, the final deflection circuit is shown. In order to interrogate a particular address, the binary code representing this address is transferred broadside to a deflection register. Nine of the 12 binary stages of the deflection register are connected to the deflection system by 9 address lines only one of which is shown in Figure 10. The deflection system, exclusive of the deflection register, is located in the electrostatic memory frame. The voltage of these address lines is either at +10 or -30 volts, depending on the signal being transmitted. In Figure 10 an address line is connected to a typical channel. The purpose of such a channel is to move the beam 1, 2, 4, 8 or 16 increments. An address line is directly coupled to the phase inverter which drives the cathode followers. The push-pull signals from these cathode followers drive the current switch tube so that the current, I_p, is made to flow through either the left half or the right half of this tube. The magnitude of the current, I_p, is determined by the value of the resistor, R_k, and the voltage to which it is returned. The resistance, R_k, is large enough so that the variational impedance, as measured at the plate of the current switch tube is much larger than the plate impedance. This causes the plate current, I_p, to be nearly independent of the voltage appearing at the plate of the current switch tube.

In this way the currents flowing in the left half of the current switch tubes add in the summing resistor, R_s, without interaction. The only difference existing between the various channels is the value of R_k, and the number of tubes used in the current switch. It was our experience that the bias changes, due to different values of R_k, had a negligible effect on the accuracy of beam positioning. Neglecting corrections for tolerance build-up, the values of the resistors, R_k, form a geometric progression. Thus the plate currents switched by the various channels is I_p, 2 I_p, 4 I_p, etc. By changing the value of the resistor, R_c, the magnitude of the beam deflection for a given value of I_p can be changed without changing the average voltage of the horizontal deflection plates.

In the first design of the deflection system, type 807 tubes were used as the output cathode followers. These were rejected because microphonism caused errors in the operation of the electrostatic memory. For a period of about two months, 30 random errors were detected of which all were at addresses along one edge of the raster. Replacement of the 807's with 5965's eliminated this random error difficulty. Since this change, no errors which could be attributed to microphonics have been detected. Furthermore, the deflection circuits are insensitive to mechanical shock and vibration.

In the design of this deflection circuit, careful consideration was given to its speed of response. When a high read-around ratio is required, it is very important that the beam be unblanked so that it bombards an address with a displacement error no larger than about 0.1 of a beam diameter. In other words, this digital to analog converter must have an ability to be reset within 0.05%.

Experimentation showed that a linear sweep of the dash generating deflection voltage produced a larger dash signal than a step wise positioning of the beam. In addition to a larger dash signal, the linear sweep produced more uniform dash signals. The dash generator, shown in Figure 11, produces a linear sweep at the deflection plates during dash unblank time. The "switching circuits" determine in which direction the beam is to be deflected. This is necessary because in the raster layout, the tails of the dashes point in opposite directions in alternate rows. The dash generator consists of two cathode followers driving a cathode coupled amplifier. If a negative pulse is applied to the grid of the left cathode follower, this cathode follower will be cut off. The potential of its cathode and hence the potential of the corresponding grid of the cathode coupled amplifier will start to decrease linearly with time. The plates of the cathode coupled amplifier supplya push-pull signal which is attenuated by means of the resistors, R_a, and is coupled by them to the plates of the current switch tubes. If the beam of a cathode ray tube is unblanked at the time the negative pulse is applied to the grid of the cathode follower, a dash will be written into this tube. When the negative pulse returns to +10 volts, the cathode follower will very quickly return the grid of the cathode coupled amplifier to its steady state value.

POWER SUPPLY STABILITY

The problem of power supply stability is a rather critical one. It must be made clear that a supply that is adequate for the major portion of a digital calculator may not be good enough for the electrostatic memory. This is especially true when a high read-around ratio is required. When a particular address in a cathode ray tube is being spilled into from an adjacent address, a dot signal from the first address will evidence jitter. This jitter will disappear when the voltages that power the deflection system are free from noise. It is the jitter of the dot signal that can drastically reduce the read-around ratio of a particular cathode ray tube, or electrostatic

memory system. It is for this reason that well-regulated supplies are used in the deflection system.

A NEW EFFECT

A source of trouble that can easily be misinterpreted as spill was discovered by W. J. Deerhake and G. F. Bland of the Watson Scientific Computing Laboratory. This effect has been given the name "mudhole". "Mudhole" arises when a particular region of the phosphor, under bombardment by the beam, acquires a higher conductivity than that of an unbombarded region. The "mudhole" characteristics of a particular tube may be checked in the following way: Write several hundred dots in rapid succession, at a particular address on the face of a cathode ray tube. Shut the beam off and even deflect it away from this address to insure that there is no beam hitting the area in question. Leave the beam off for 10 or 20 milliseconds and observe the amplitude of the dot signals obtained from this address when the beam is made to refer to it again. If "mudhole" is present, the first dot signal will be smaller in magnitude than the succeeding dot signals; it may even be positive and could be interpreted as a dash. The effect of "mudhole" is made worse by a large number of references in a short time followed by a long wait period. It has been our experience that a calcium tungstate phosphor gives relatively large dash signals and is reasonably good with respect to "mudhole". It is, however, poor for visual observation.

OVERALL OPERATING EXPERIENCE

While our operating experience is not as extensive as we would like, some of the results achieved will be presented. Throughout the testing of this memory frame our philosophy has been that it be treated like any other piece of electronic equipment, that is to say, the machine is turned on shortly before it is to be used and it is turned off during idle periods. After the "power on" switch is depressed, power is applied to the heaters of all tubes. The d-c supply voltages are applied in sequence and are made to increase in magnitude uniformly from zero. The time required between the depressing of the "power on" switch and when all voltages are stabilized is five minutes. Shortly after all the voltages have been applied the machine is ready to perform useful work. In order to remove a memory drawer it is necessary to shut down only d-c portion of the power supply. A memory drawer is removed only after the drawer in question has definitely been shown to be a source of trouble.

In order to check the drawers, the memory is periodically subjected to tests. These tests are applied to memory by means of diagnostic programs which are written specifically to check the condition of the cathode ray tubes. In addition to these tests there are other checks which are made by means of a special tester. A typical test requires that each address in memory be subjected to a read-around ratio of 200 to 1. If any cathode ray

tube fails to pass this test because of poor spill or mudhole characteristics it is rejected. The average life of the cathode ray tube that have failed to pass this test seems to be about 2, 500 hours.

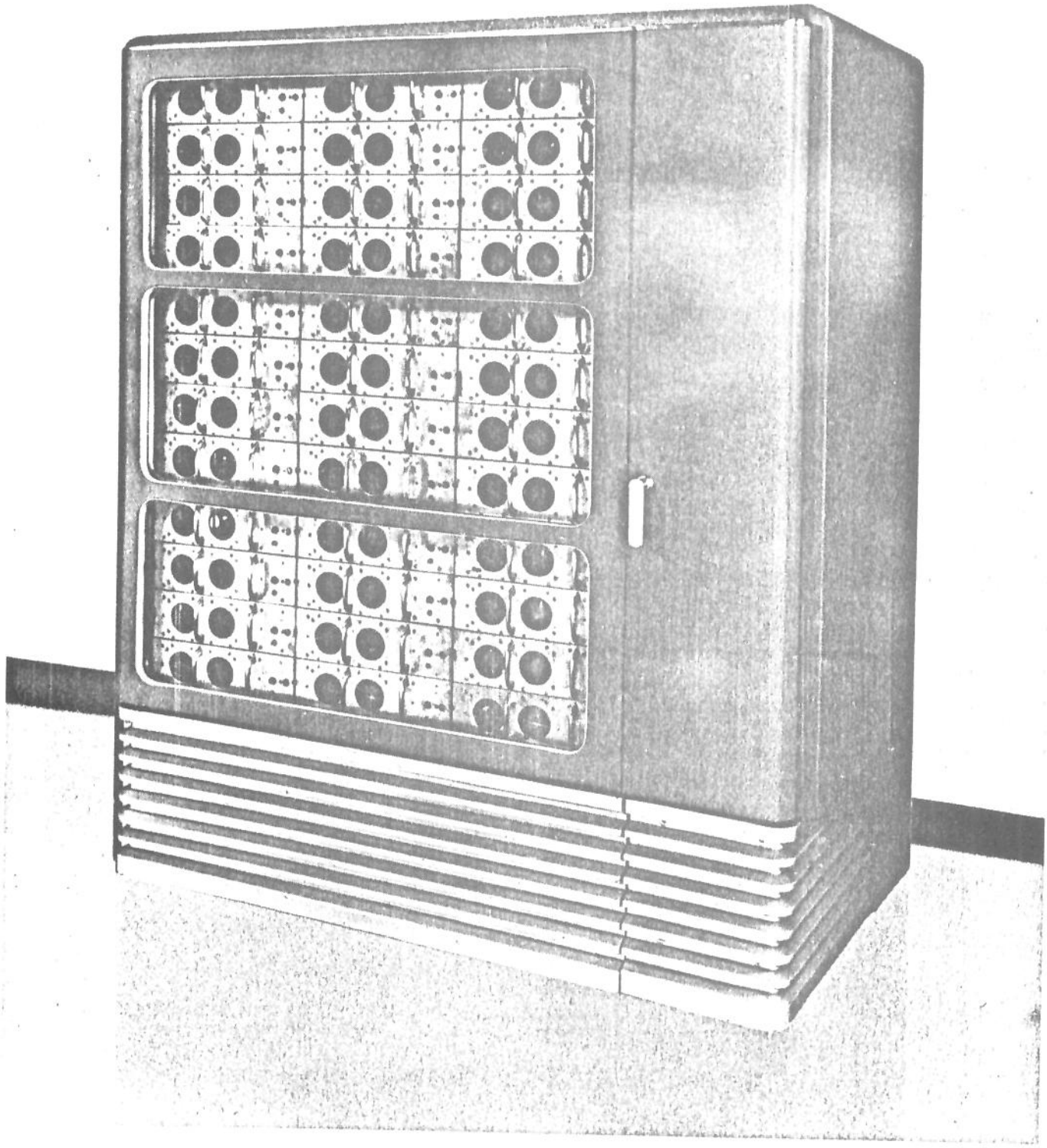
Before a cathode ray tube is rejected because of spill the memory drawer in which the tube is located is checked for alignment. This means that the dash signal is checked for intensity saturation, the beam is focused, the gain is adjusted, and the dash signal is made to coincide with the sample pulse. All of these adjustments can be made from the front of the drawer while the memory is in operation. On the average, only one memory drawer per day undergoes such adjustment.

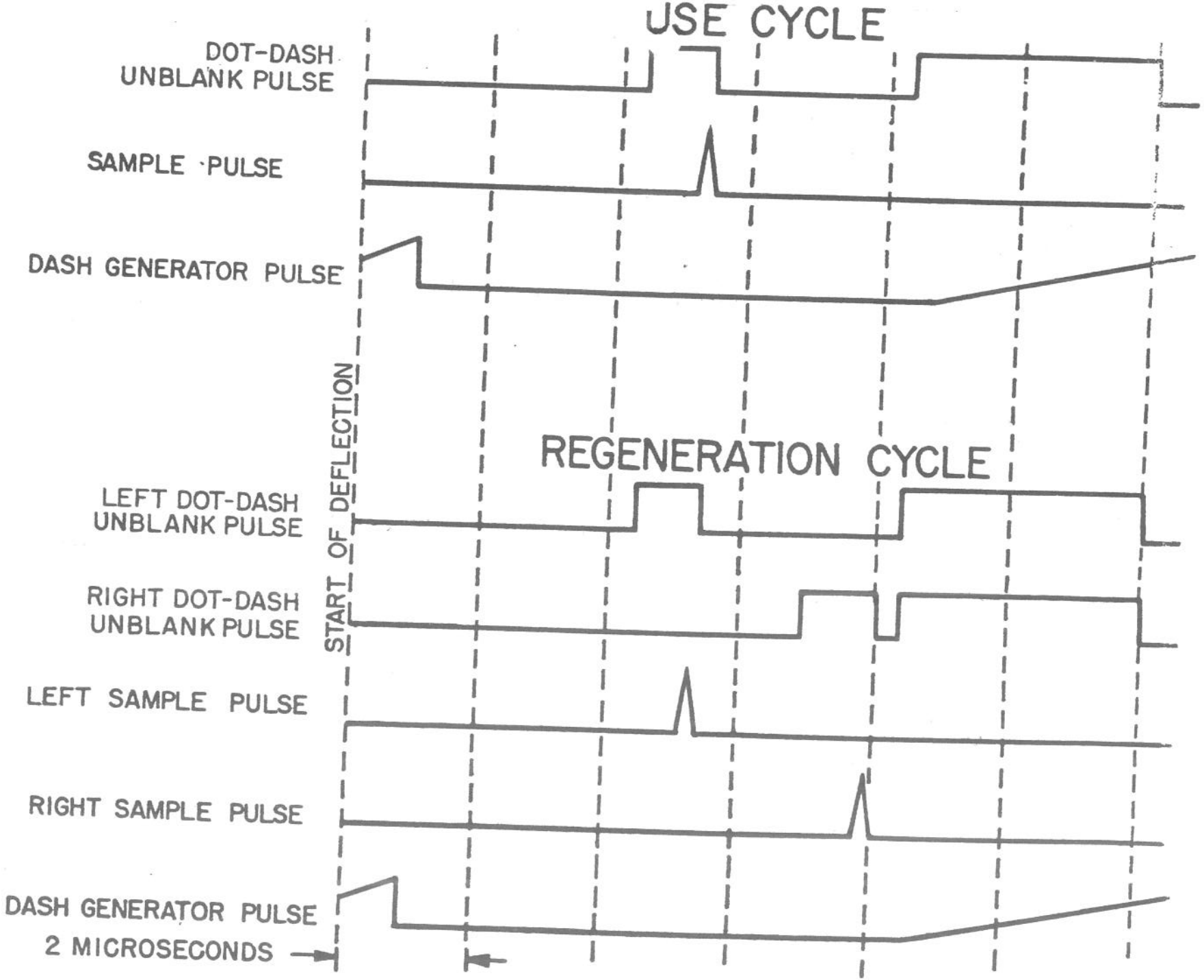
The electrostatic memory frame is rather insensitive to outside disturbances. It is subjected to mechanical impact, while the spill test is in operation, to show up microphonic tubes and poor conections. A similar test is performed electrically by requiring that the spill test run without interruption when a spark-type leak detector is operating within two feet of the memory frame. On the several occasions when memory has been checked for random errors that are generated either internally or externally, the memory has operated for eight hours without error before the test was terminated. In these tests memory operated with a read-around ratio of 100 to 1.

The memory system which has been described was designed so it could be operated with a 1, 024-bit raster as well as a 512-bit raster. A recent test has shown that satisfactory performance can be obtained with a 1, 024-bit raster. This is a rather severe test since for satisfactory performance memory must operate with a read-around ratio of 400 to 1. We feel this type of operation in addition to its reliability and ease of maintenance has established cathode ray tube storage as a very satisfactory memory system.

RECOGNITION

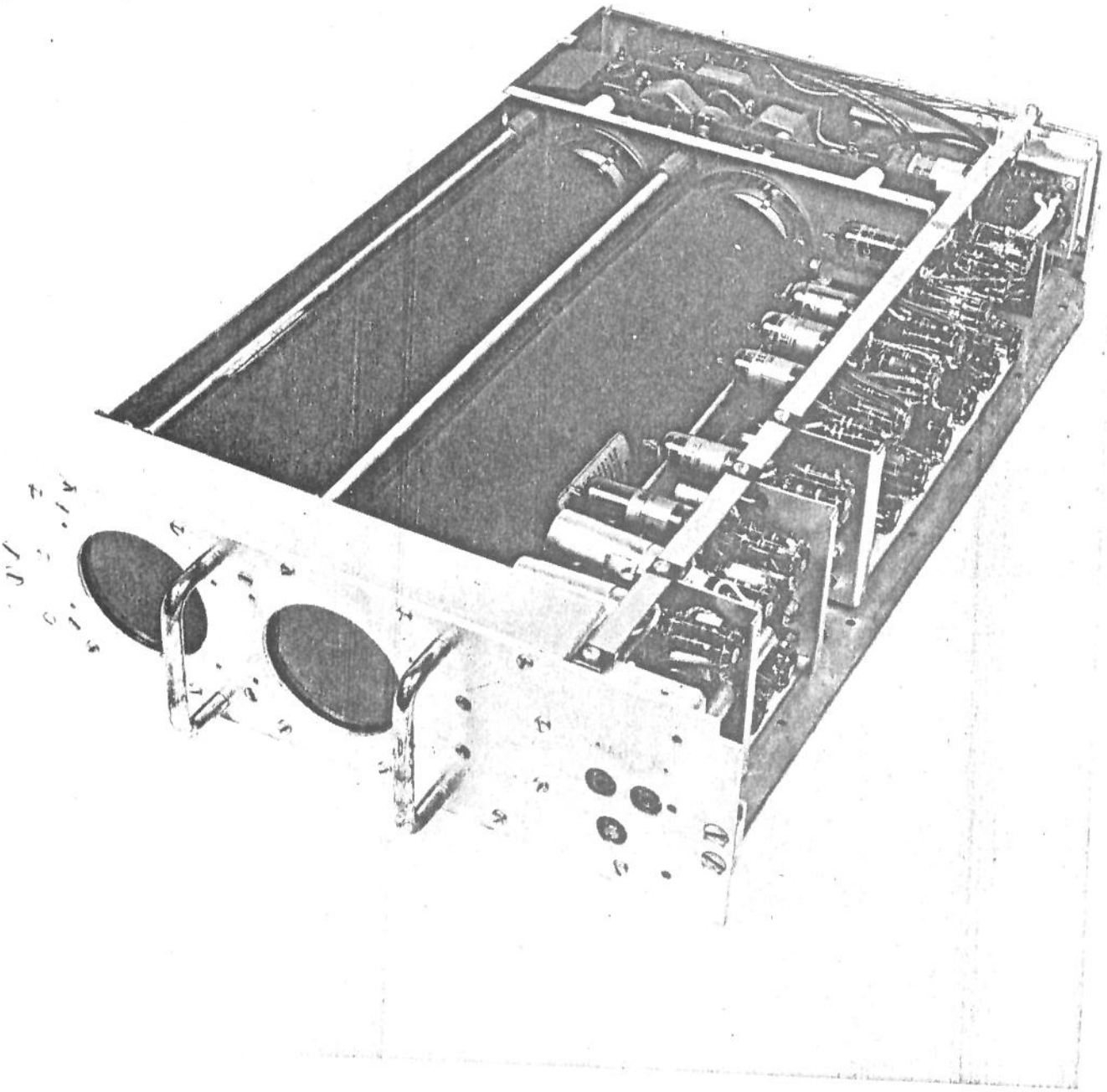
In closing, we wish to thank J. A. Haddad, P. E. Fox and the many people who have contributed in designing, constructing and putting this machine into production. Without their help, this paper would not be possible.

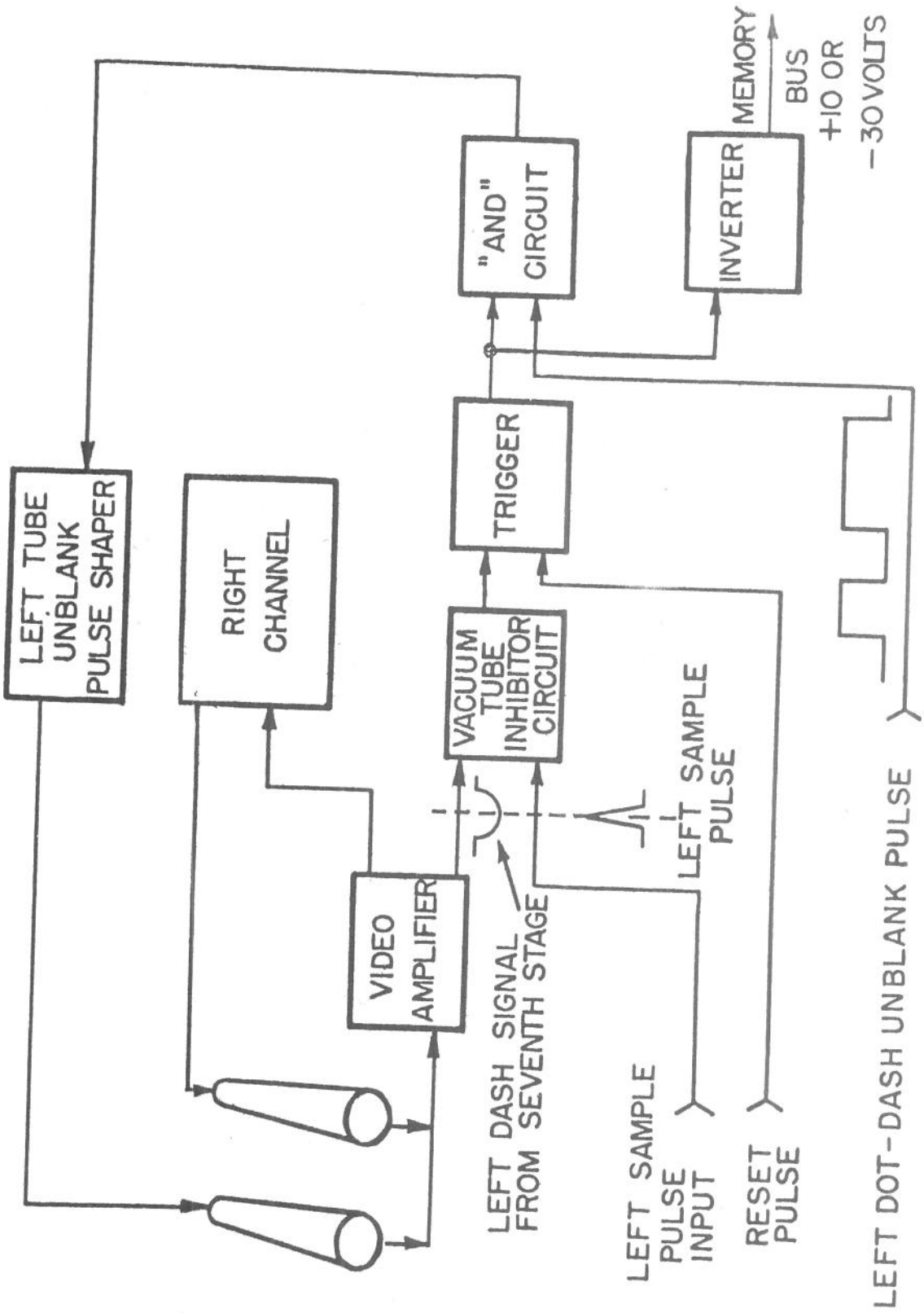




CYCLE TIMING DIAGRAM

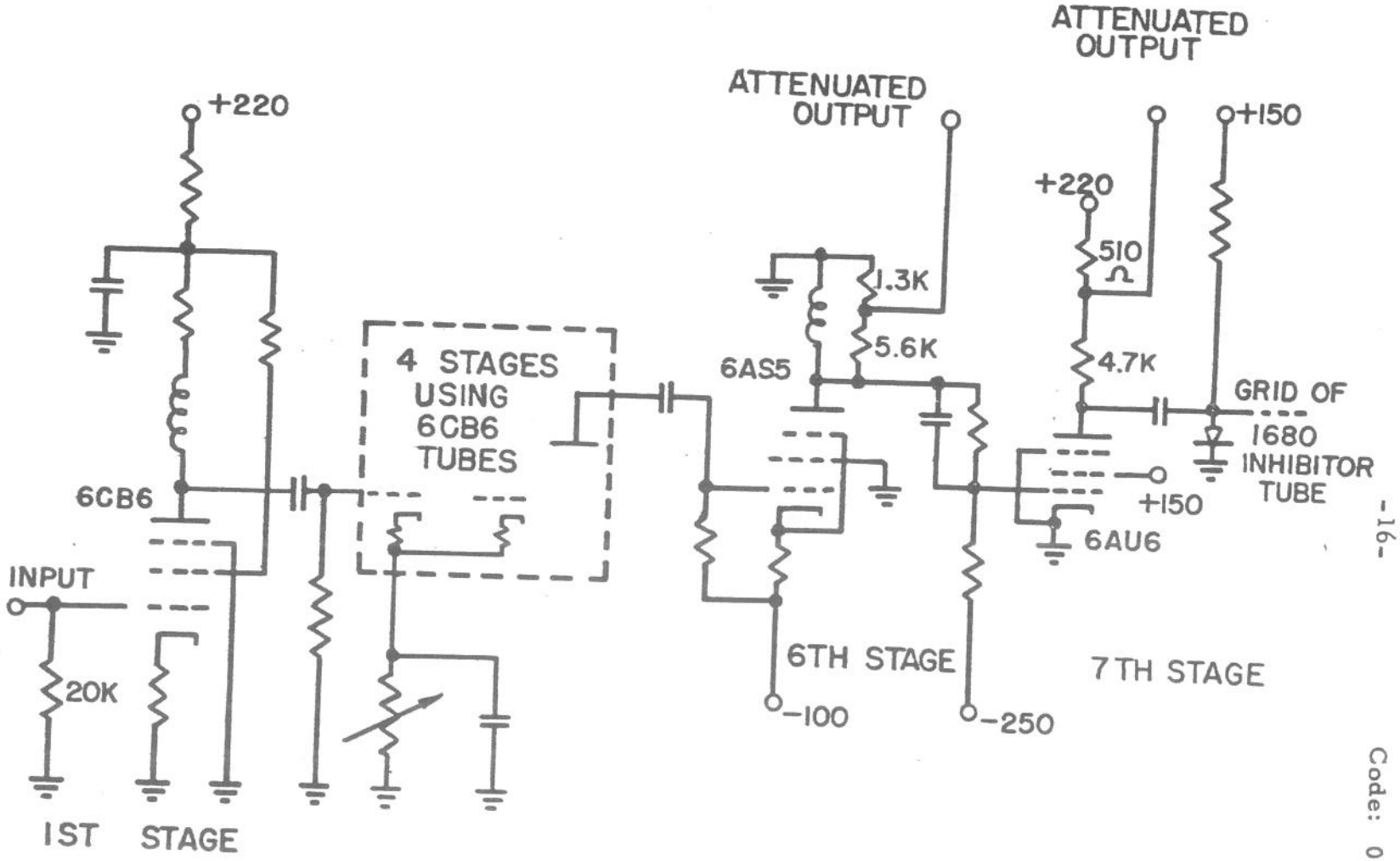
FIGURE 2





SIMPLIFIED BLOCK DIAGRAM OF MEMORY DRAWER

FIGURE 4



VIDEO AMPLIFIER SCHEMATIC

FIGURE 5

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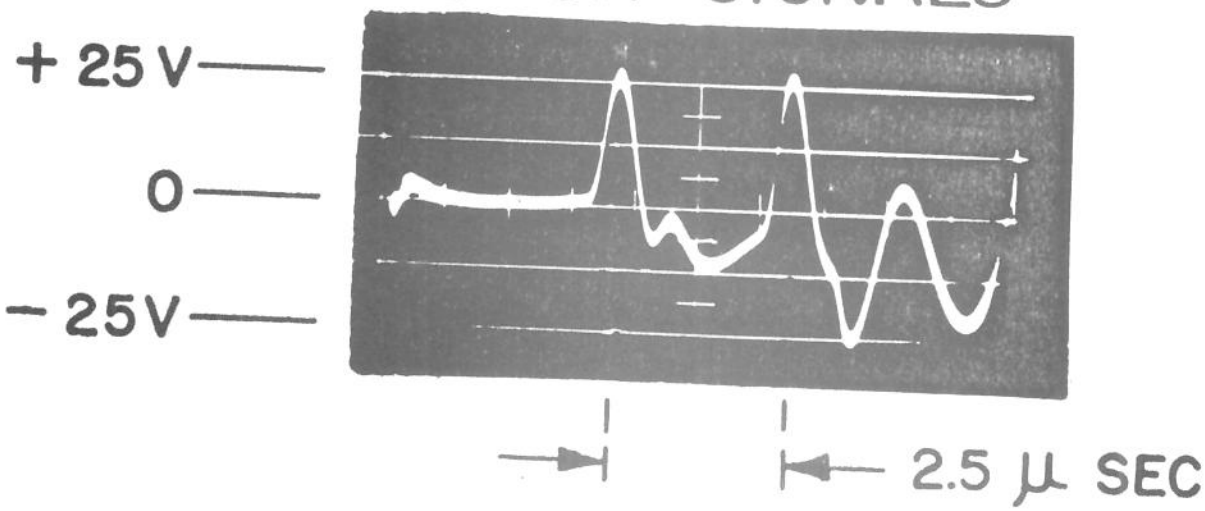
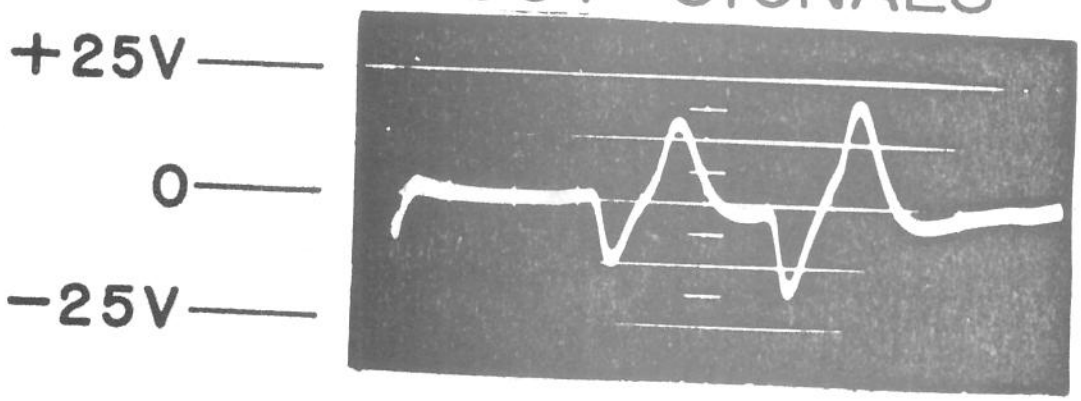
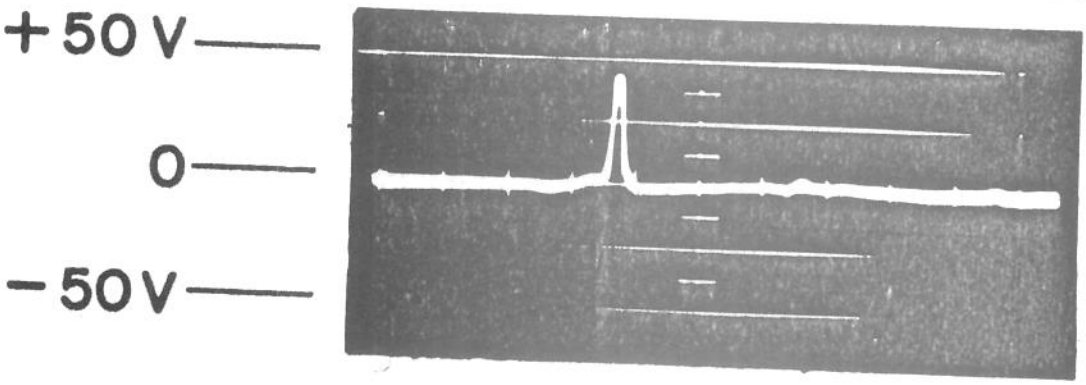
DASH SIGNALS

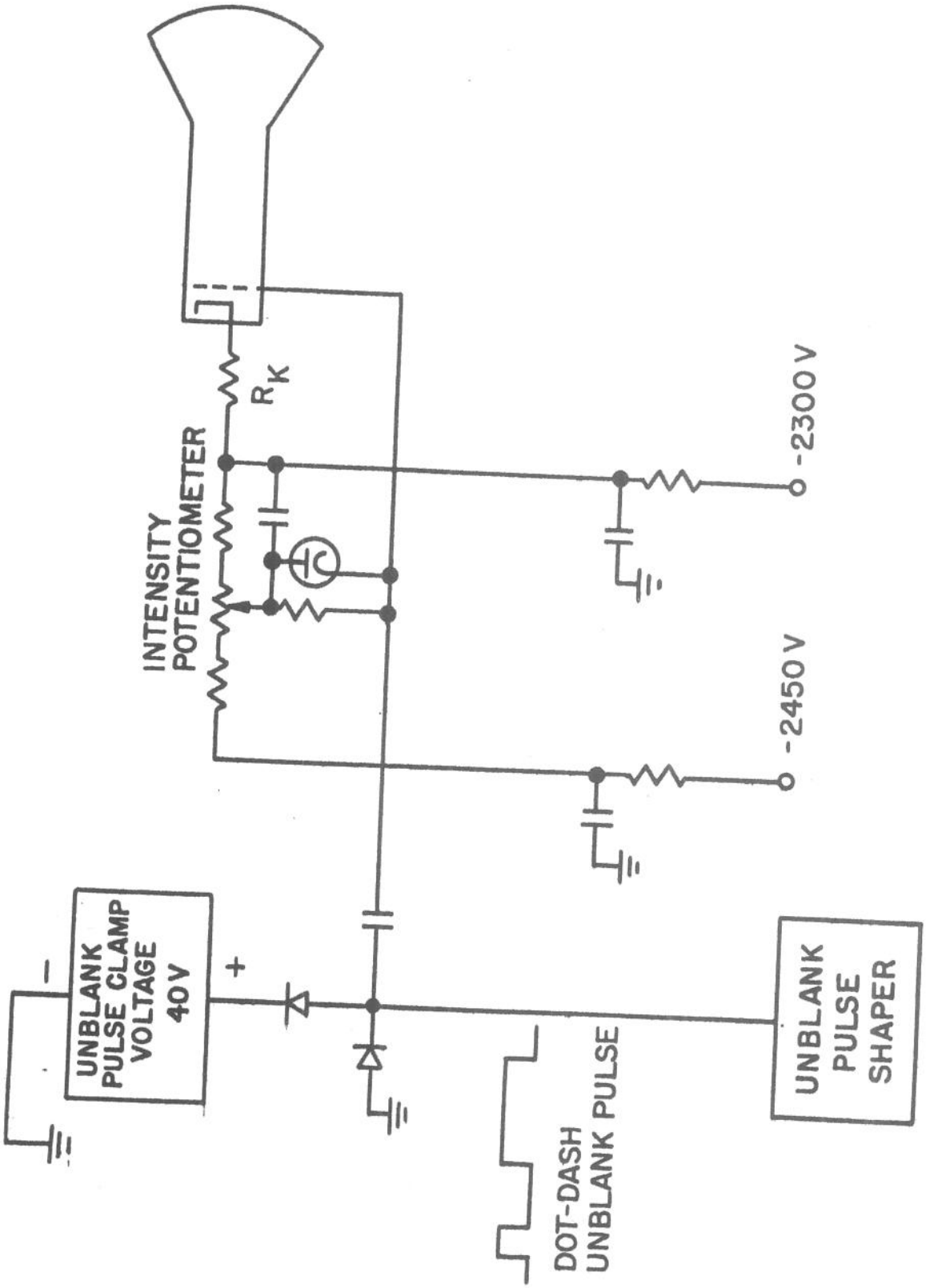


DOT SIGNALS



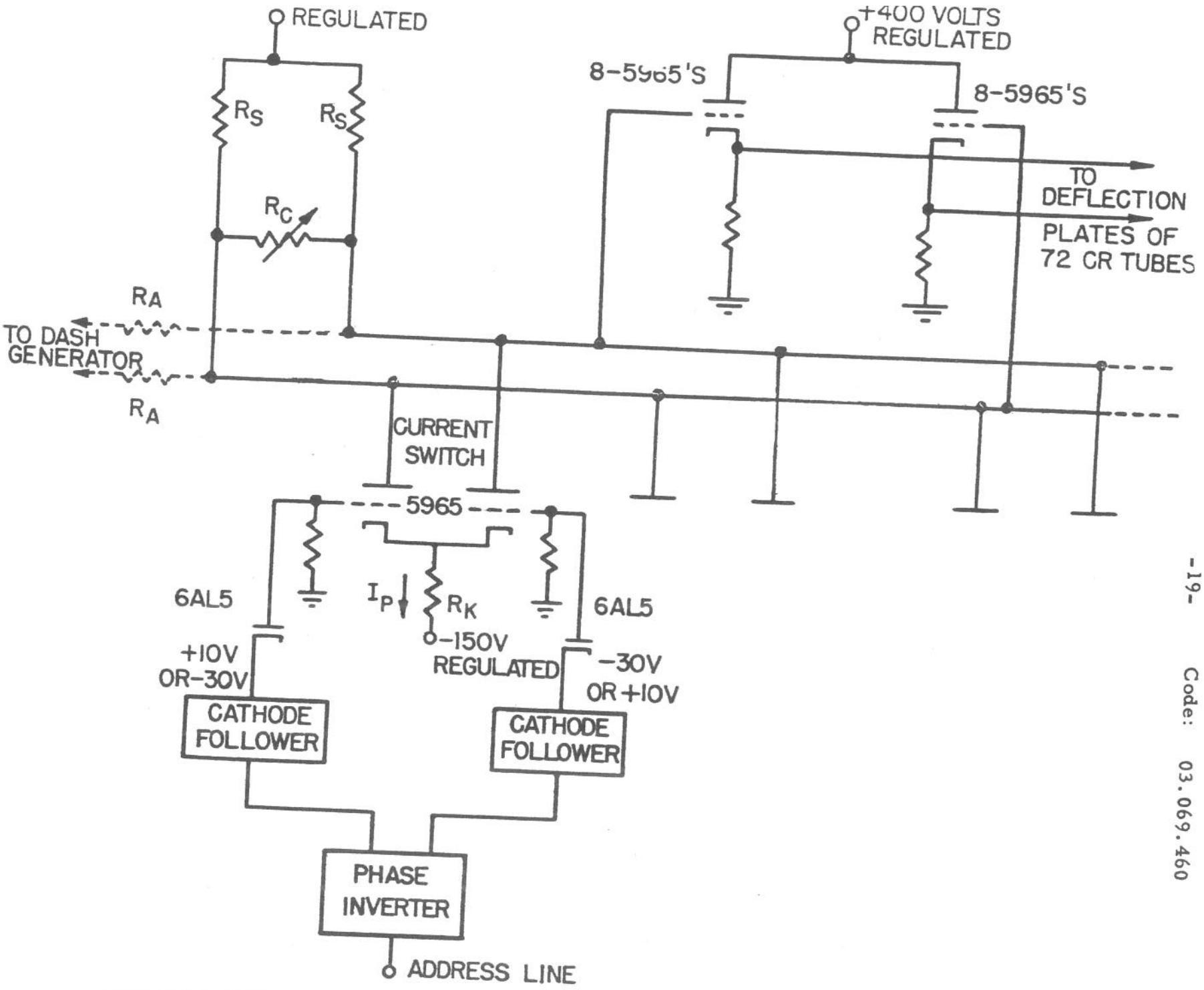
LEFT SAMPLE PULSE





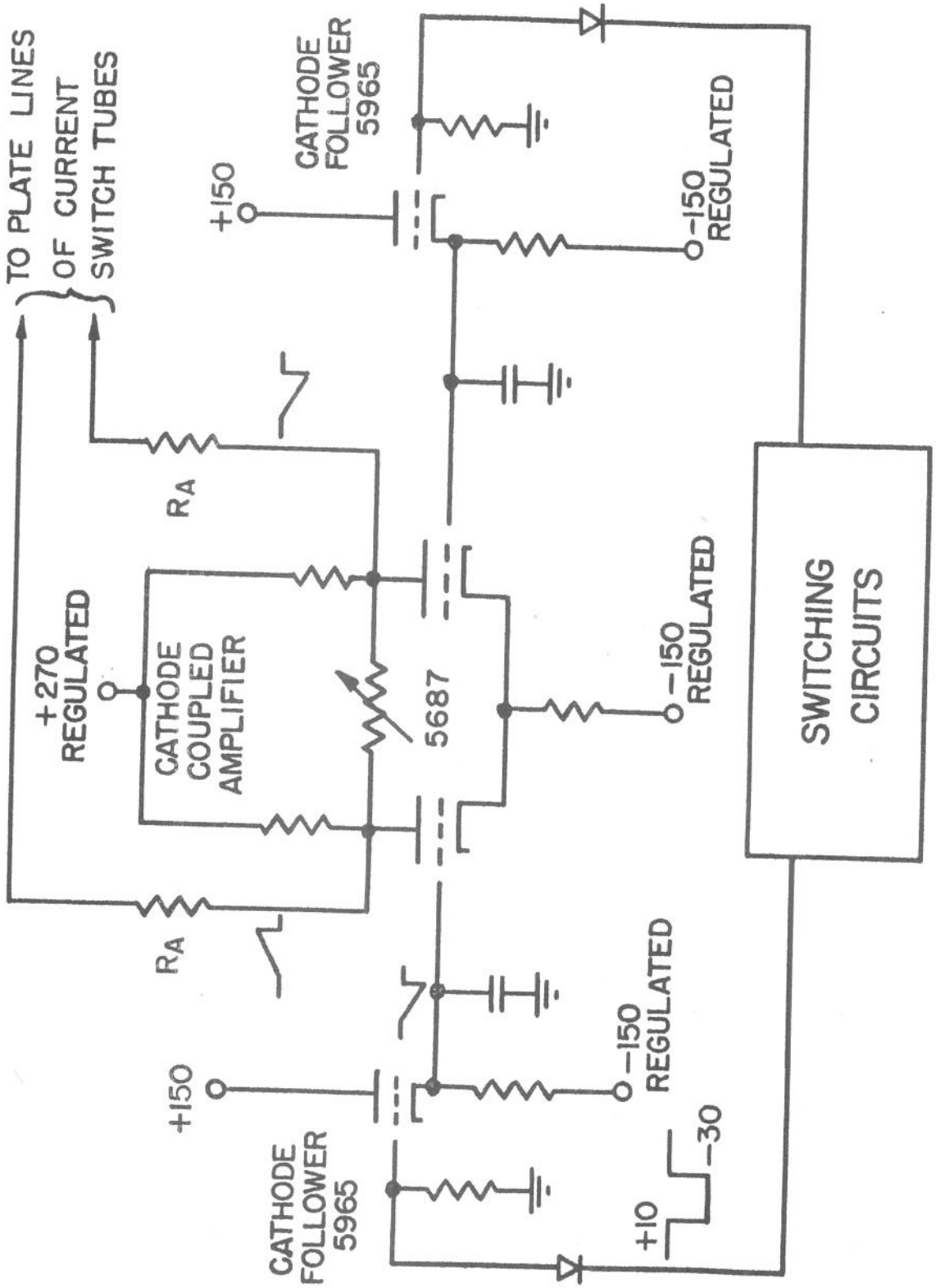
CRT UNBLANK CIRCUIT

FIGURE 8



SIMPLIFIED HORIZONTAL DEFLECTION SYSTEM

FIGURE 12



DASH GENERATOR

FIGURE 11